A Translator Verification Technique for FPGA Software Development in Nuclear Power Plants

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Introduction (1/2)

NuDE 2.0
Introduction (2/2)

Verifying ‘FBDtoVerilog’

• Co-Simulation technique can be used for demonstrating the correctness of translator such as ‘FBDtoVerilog’
• For this co-simulation technique, many tools run separately such as ‘Scenario Generator’, ‘FBD Simulator’
• We had develop integrated tool to support the co-simulation
Background (1/3)

FBD Simulator

- Simulator for FBD
- Automatically classifies the POU (Program of Unit) in the FBD
- It presents input, output and local variable lists
Background (2/3)

Scenario Generator

• A tool that automatically generate an infinite number of scenarios
• Input is FBD
• It reflects the features of the domain such as range of value
Co-Simulation

- Indirect verification technique
- It simulates programs with same scenario and compares results of simulation for confirming correctness
- Confirmation of correctness with co-simulation can make to enhance the reliability of the program
The Integrated Tool for Demonstrating the Correctness of Translator

Overall Process – Before Using Integrated Tool

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<tr>
<th>Translators</th>
<th>Programs</th>
<th>Scenario Generation</th>
<th>Simulation Tools</th>
<th>Simulation Results</th>
<th>Comparison</th>
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</thead>
<tbody>
<tr>
<td>FBDtoVerilog2.0</td>
<td>FBD</td>
<td>Scenario Generator</td>
<td>FBD Simulator</td>
<td>FBD Simulation Result</td>
<td>Correct</td>
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<td>Verilog</td>
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<tr>
<td>Commercial Synthesis Tools</td>
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<td>EDIF Simulation Result</td>
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<td>Verilog Simulation Result</td>
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<td>Comparator</td>
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</tbody>
</table>

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The Integrated Tool for Demonstrating the Correctness of Translator

Overall Process – Using Integrated Tool
The Integrated Tool for Demonstrating the Correctness of Translator

Input programs

- FBD
- Verilog
- EDIF
The Integrated Tool for Demonstrating the Correctness of Translator

Scenario Generation

- Use ‘Scenario Generator’
- Create script (.do file) for automatically use of ModelSim
The Integrated Tool for Demonstrating the Correctness of Translator

- ModelSim Script (.do file)
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Simulation & Comparison

- Simulation

- Comparison

- Result
  - Correct
  - Not Correct

→ Counter example
The Integrated Tool for Demonstrating the Correctness of Translator

- Simulation result file
## Case Study

- KNICS RPS BP

<table>
<thead>
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<th></th>
<th>FIX_FALLING</th>
<th>FIX_RISING</th>
<th>MANUAL_RATE_FALLING</th>
<th>VARIABLE_FALLING</th>
<th>VARIABLE_RISING</th>
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</tbody>
</table>

**Total 5000 scenario / All Correct**
Conclusion and future work

• We developed the integrated tool in order to automatically perform the co-simulation
• We demonstrated the correctness of translator
  • ‘FBDtoVerilog2.0’
  • ‘Synplify Pro’

• We plan to extend the integrated tool to verify VHDL
• And plan to elaborate the scenarios on the basis of adequate coverage criteria in order to increase the confidence of verification
THANK YOU