

# RM+ / SA

김재엽  
정세진

1. SA
2. RM+

# INDEX

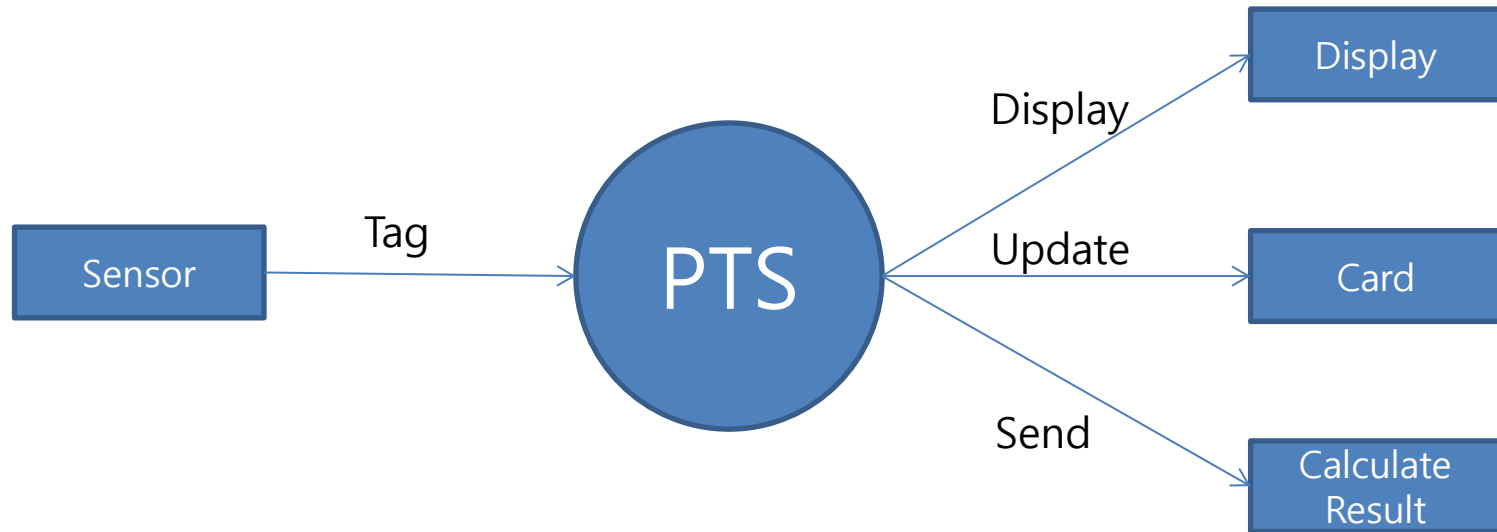
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# SA

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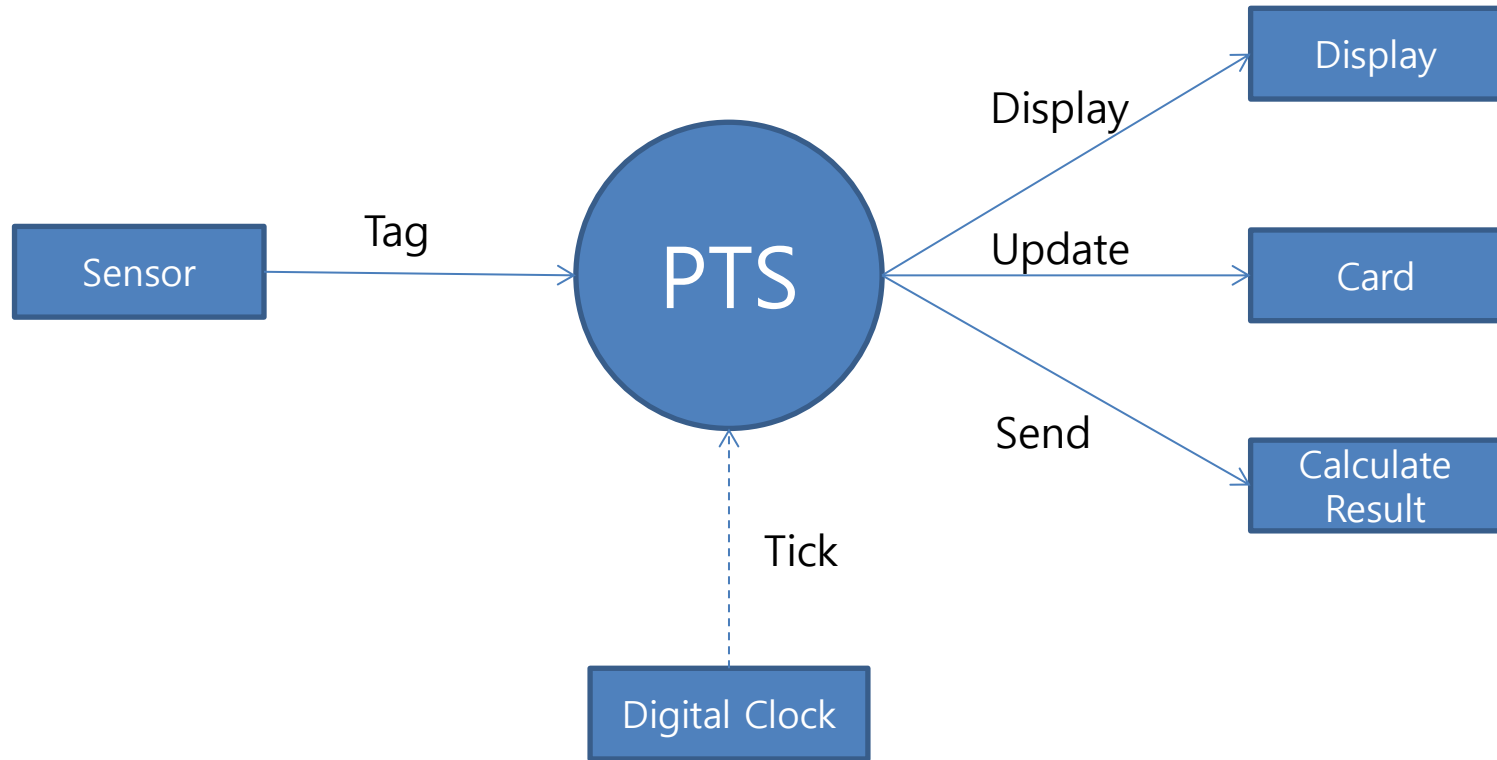
# System Context Diagram + Event List



Input / Output Event	Description
Tag	Sensing
Display	show fee, balance and time
Update	Write card information to card after fee impose
Send	Send calculate result each bus and station

# DFD Level 0

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# DFD Level 0

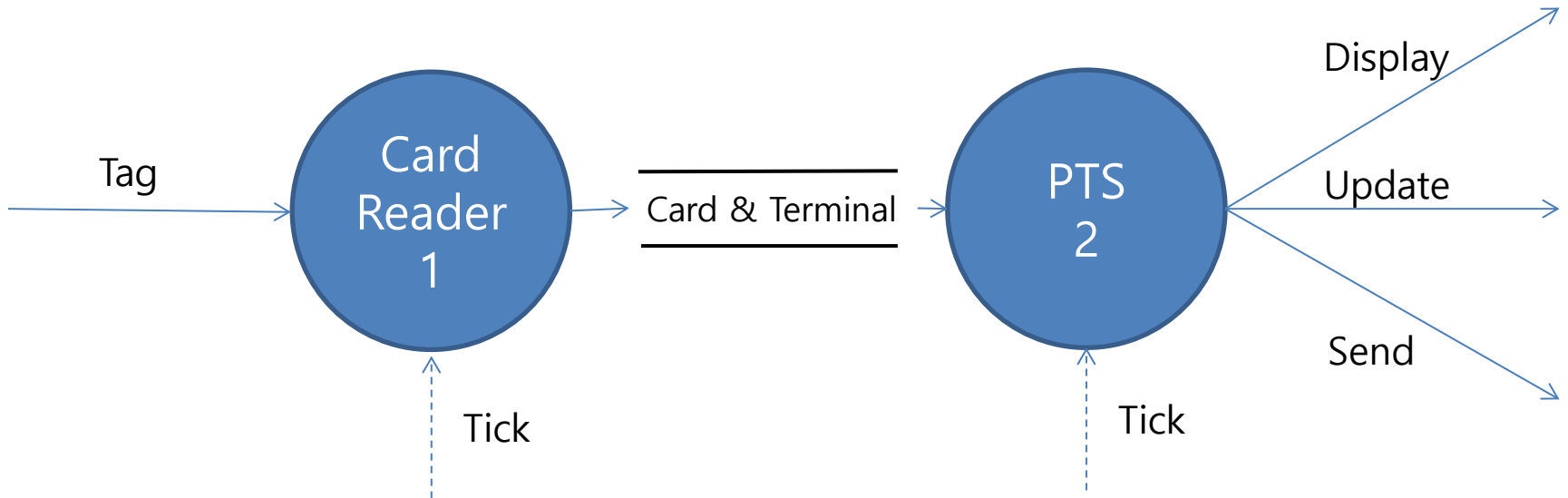
## - Data Dictionary

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Input / Output Event	Description	Format
Tag	Sensing if card is tagged	Data Structure (시간, 교통수단, 승/하차, 잔액, 업데이트 여부)
Display	Showing balance, fee, time	Data Structure (사용금액, 잔액, 시간)
Update	Writing card information to card after paying	Data Structure (시간, 교통수단, 승/하차, 잔액, 업데이트 여부)
Send	Sending result of calculate each bus/subway	Data Structure (버스 정산 결과, 지하철 정산 결과)
Tick	Digital clock has periodic tick	Periodic

# DFD Level 1

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# DFD Level 1

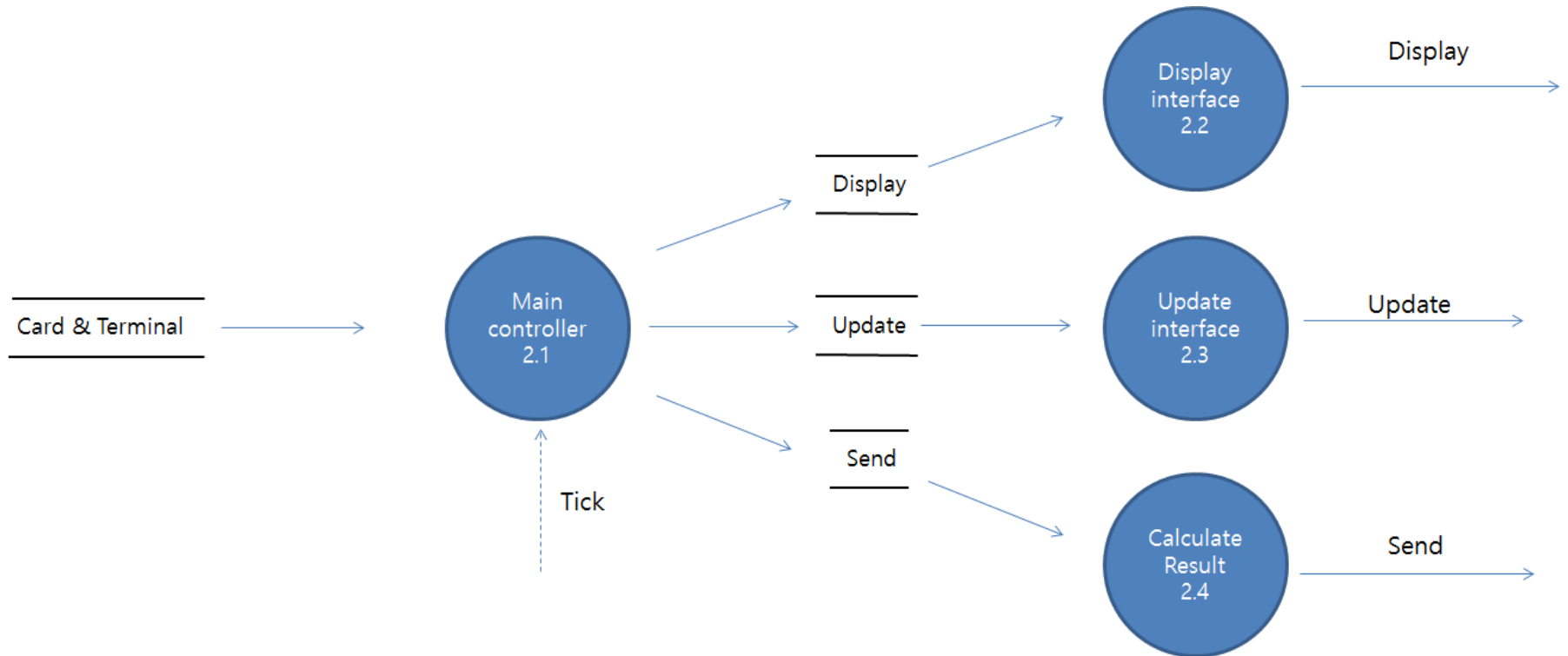
## - Data Dictionary

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Input / Output Event	Description	Format
Card & Terminal	Card information and each terminal information	Structure (시간, 교통수단, 승/하차, 잔액, 단말기 교통수단)



# DFD Level 2

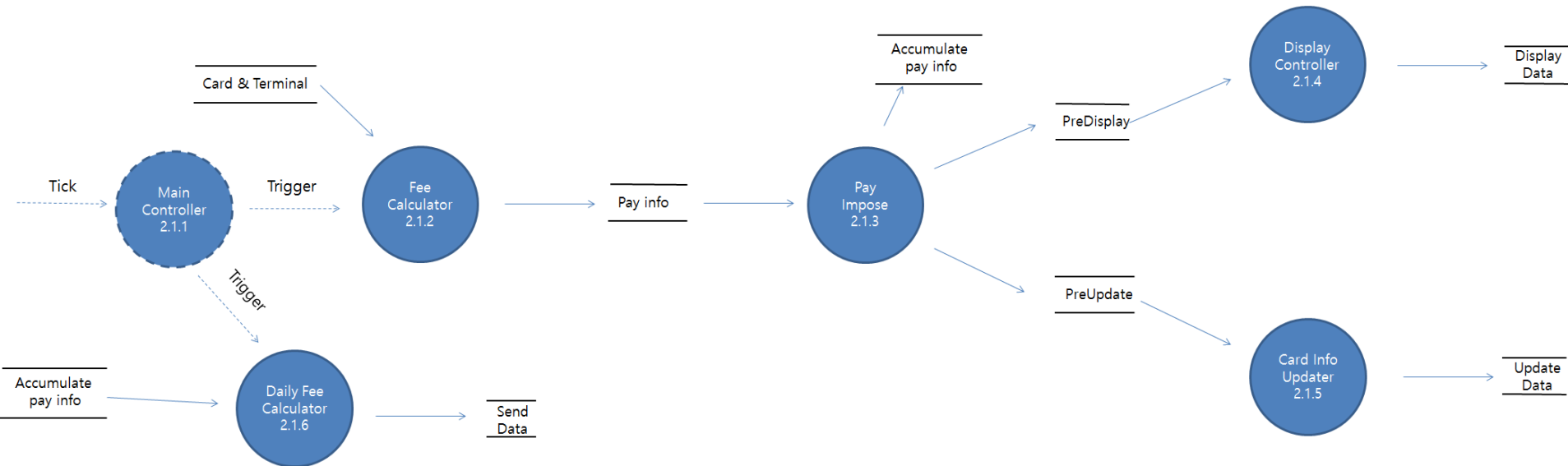


# DFD Level 2

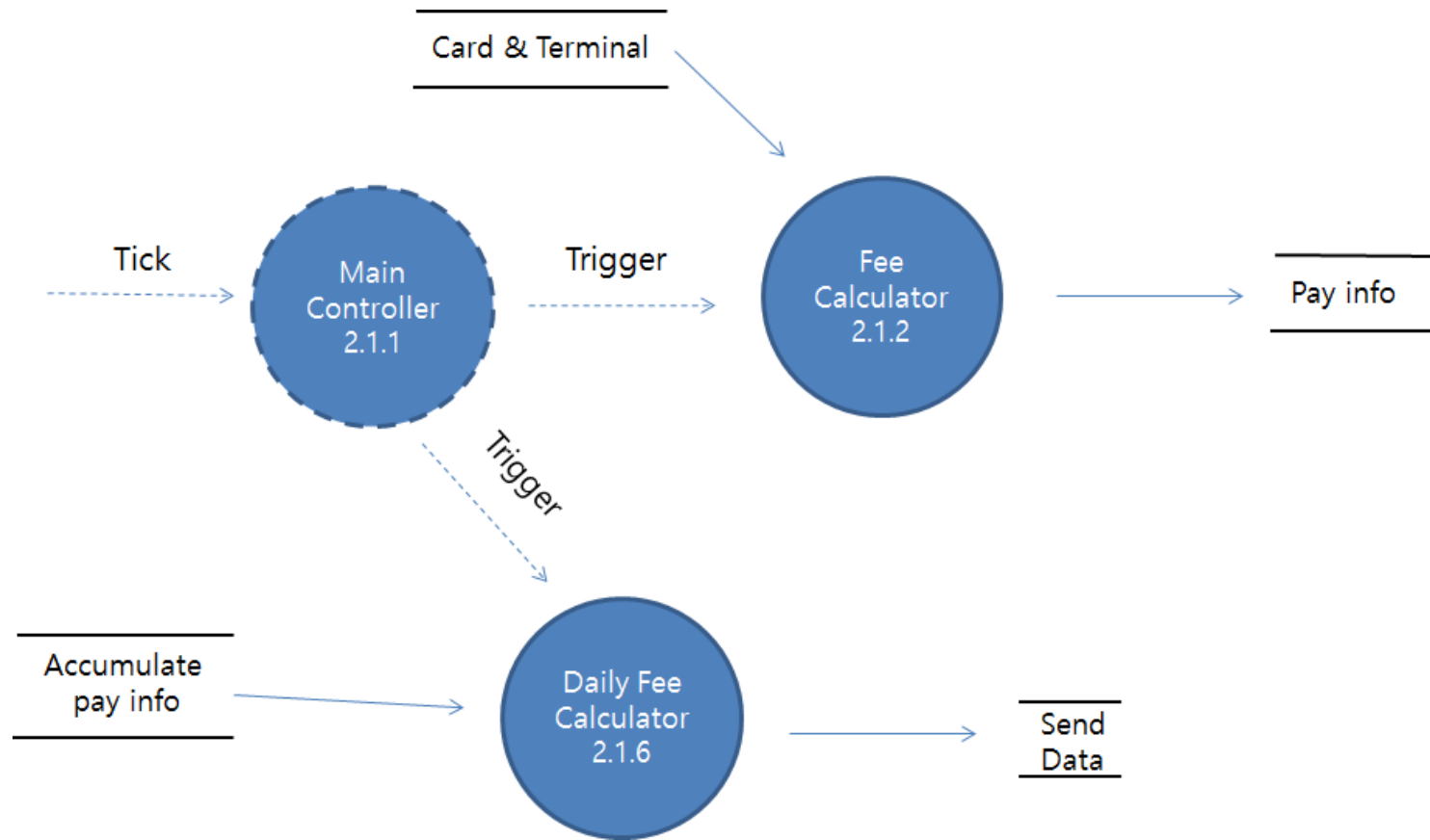
## - Data Dictionary

Input / Output Event	Description	Format
Display Data	Data for displaying terminal like Fee, balance, time	Data Structure (사용금액, 잔액, 시간)
Update Data	Data for updating card like time, balance. And it also contains update, if it is false, update is not needed.	Data Structure (시간, 교통수단, 승/하차, 잔액, 업데이트 여부)
Send Data	Result data of fee calculation about day	Data Structure (버스 정산 결과, 지하철 정산 결과)
Tick	Tick is a time data	Periodic

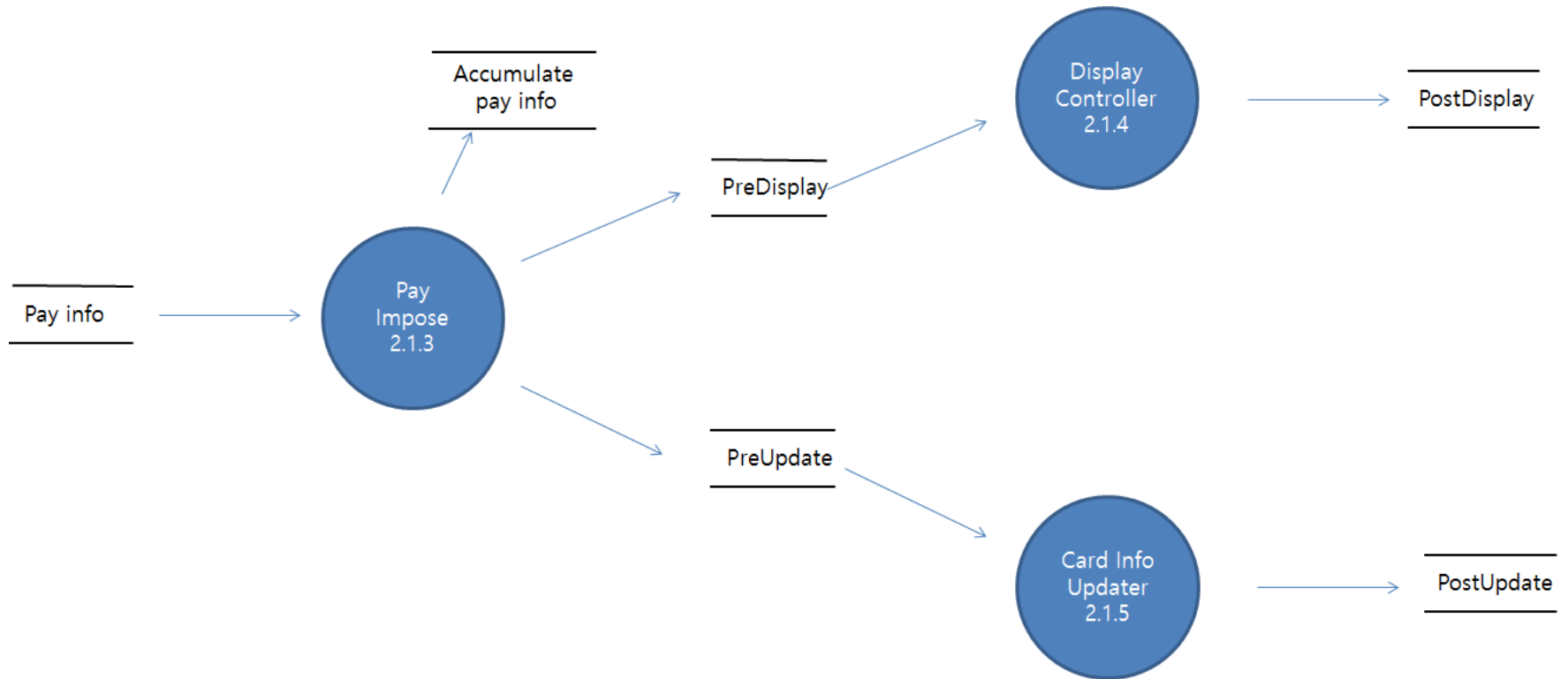
# DFD Level 3



# DFD Level 3 (Cont.)



# DFD Level 3 (Cont.)



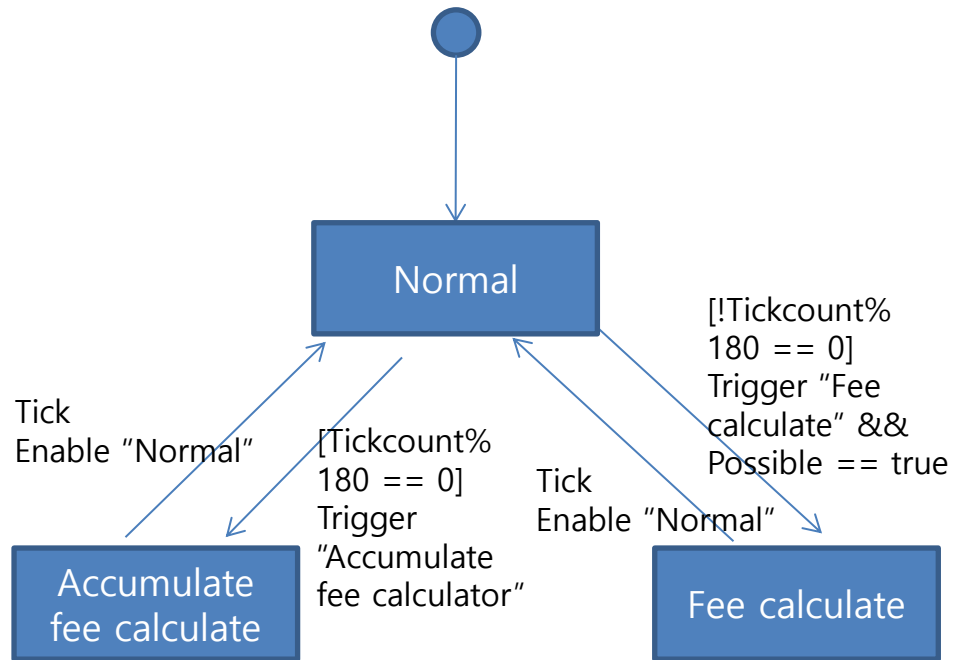
# DFD Level 3

## - Data Dictionary

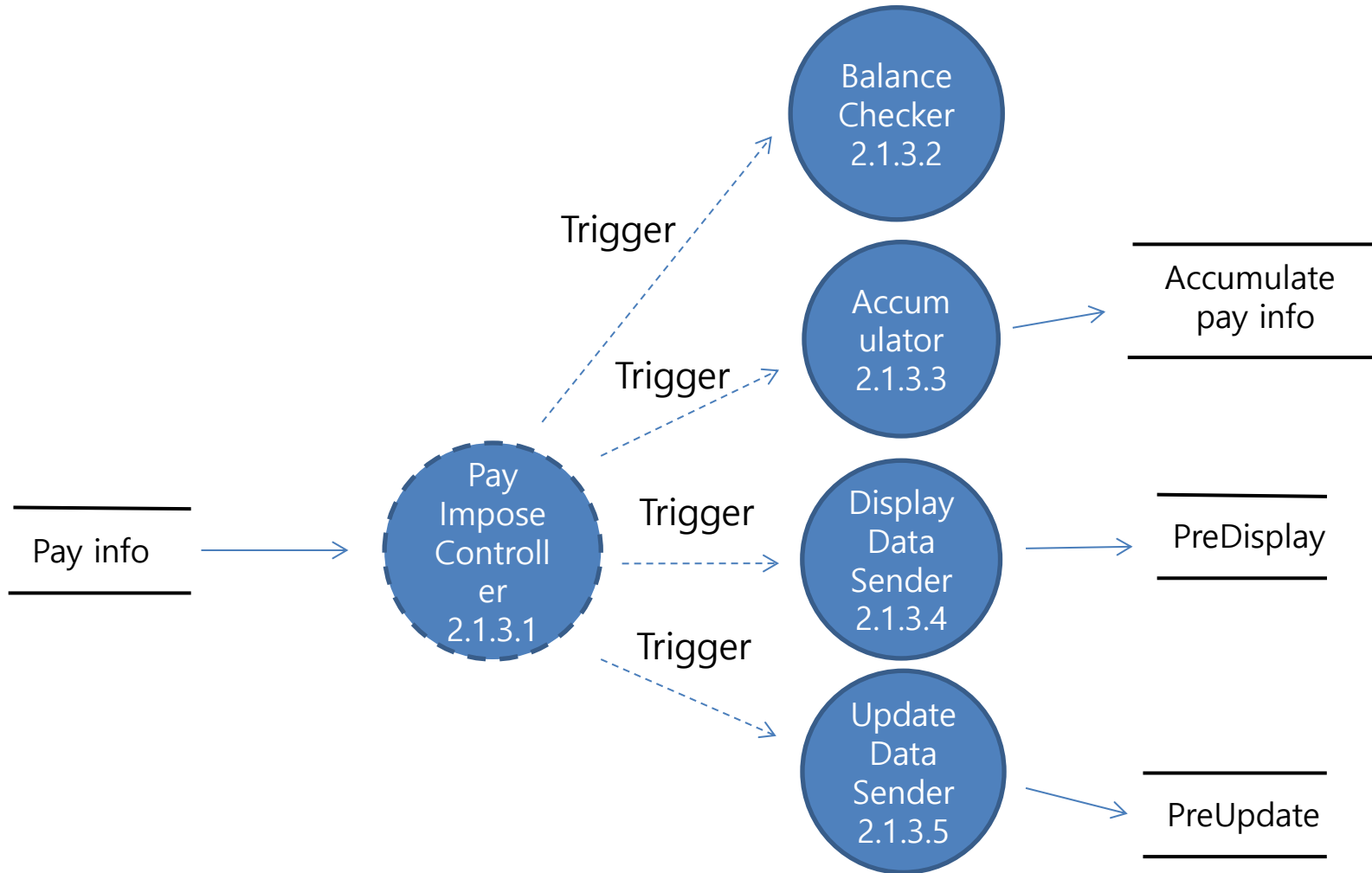
Input / Output Event	Description	Format
Pay info	Fee data for users	Structure (시간, 교통수단, 승/하차, 잔액, 단말기 교통수단, 결재금액)
Accumulate pay info	Accumulate fee data each terminal	Data Structure (누적금액, 시간, id)
PreDisplay	Data for displaying screen and terminal	Data Structure (사용금액, 잔액, 시간)
PreUpdate	Data for update card	Data Structure (시간, 교통수단, 승/하차, 잔액, 업데이트 여부)

# DFD Level 4

State Transition Diagram for Main Controller 2.1.1



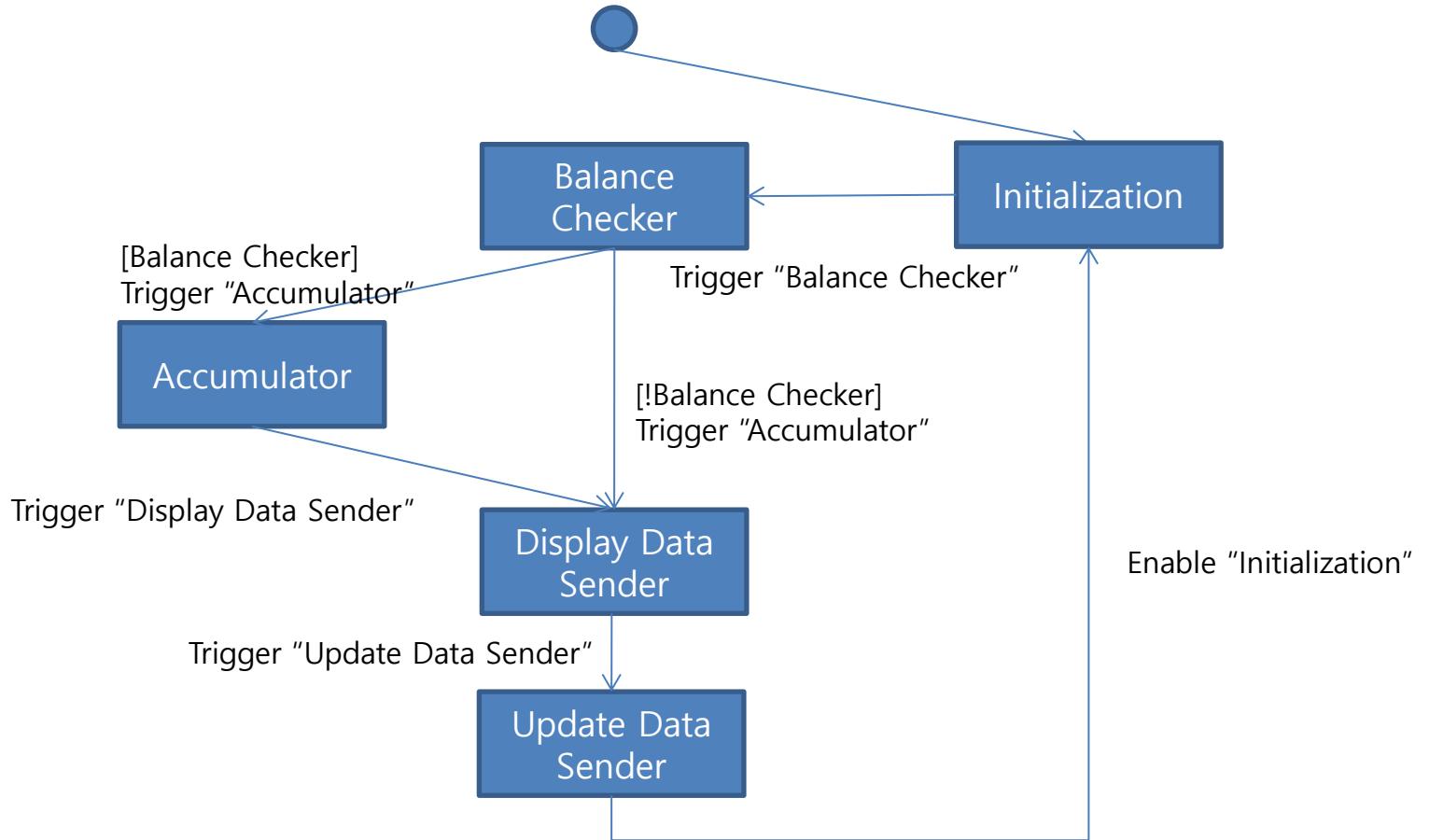
# DFD Level 4



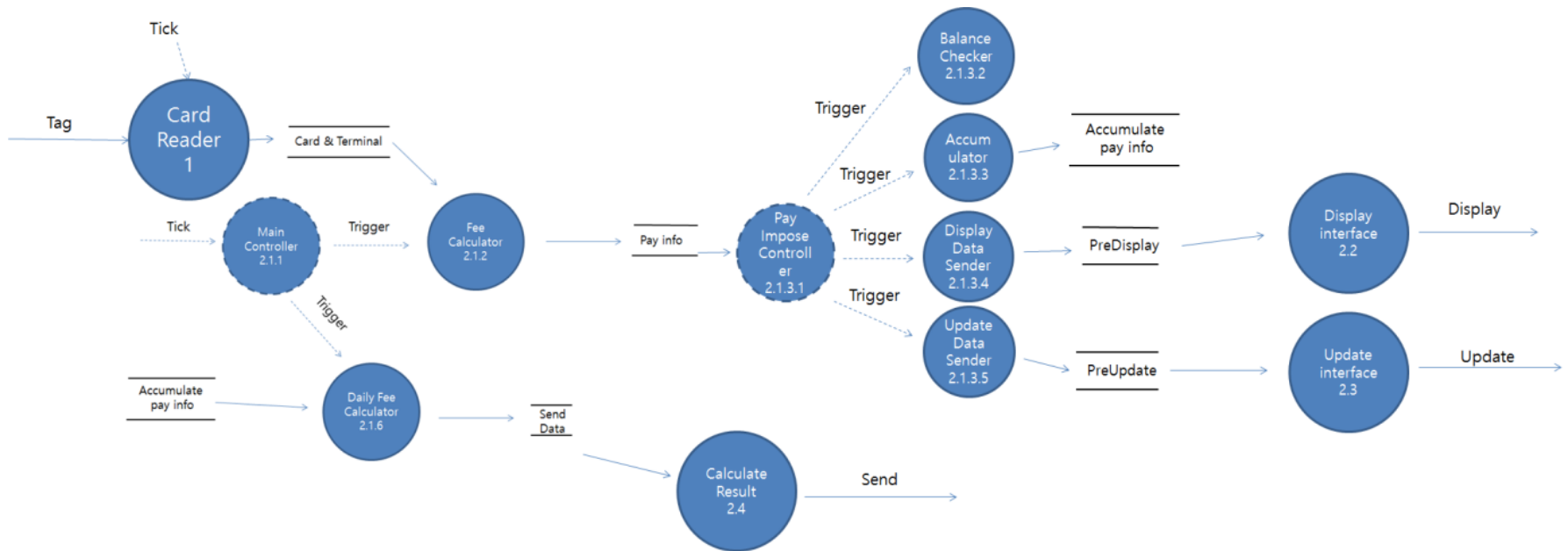


# DFD Level 5

State Transition Diagram for Main Controller 2.1.3.1



# Overall DFD



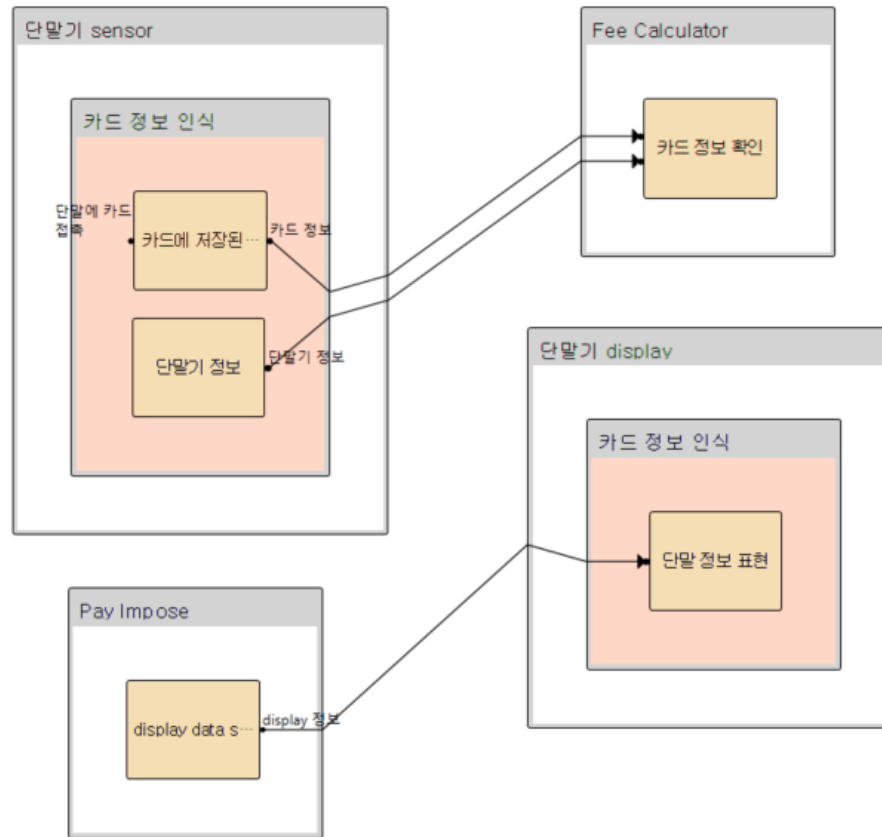
Introduce two

**RM+**

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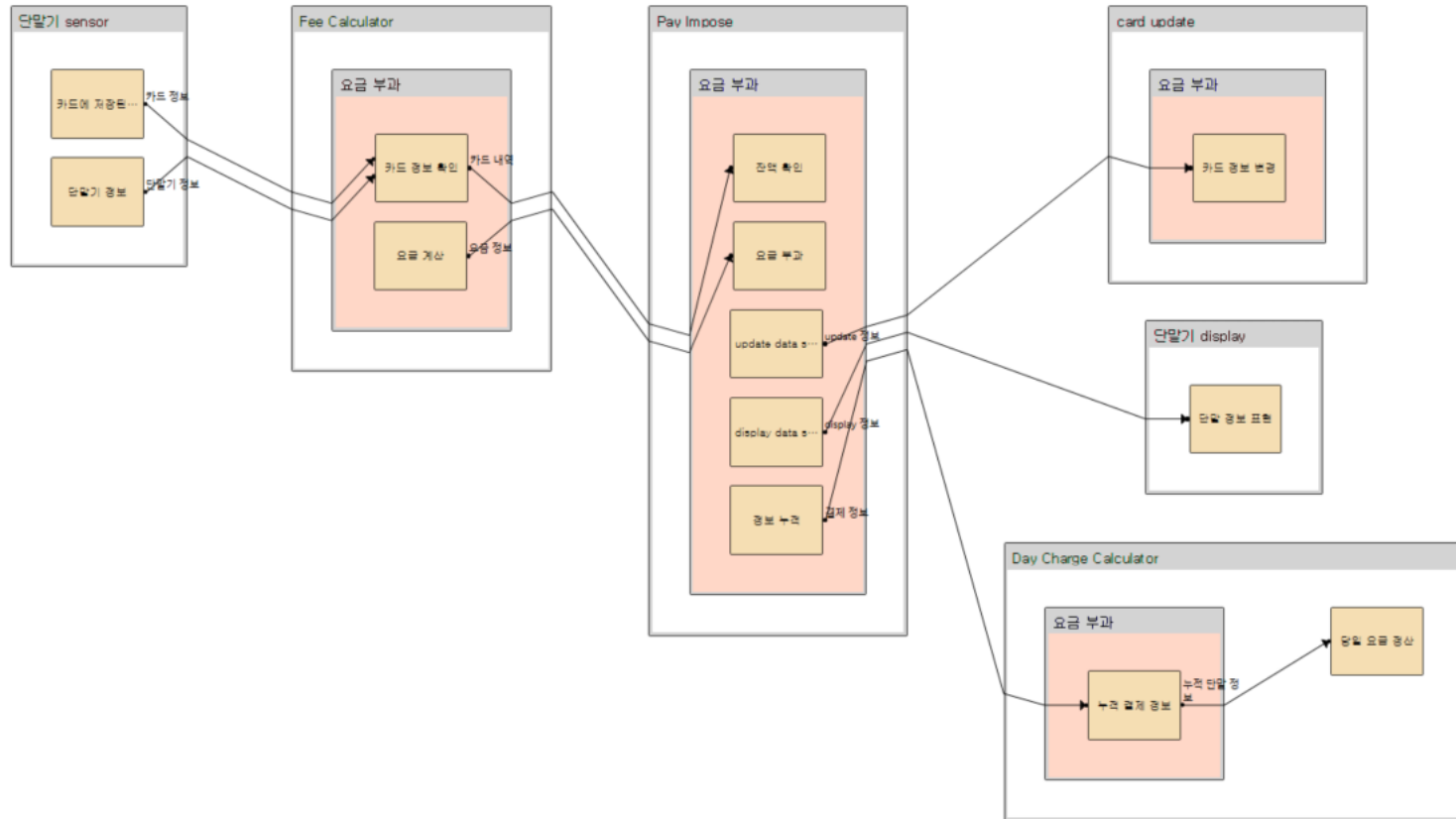
# RM+

## - Logical Design Model



# RM+

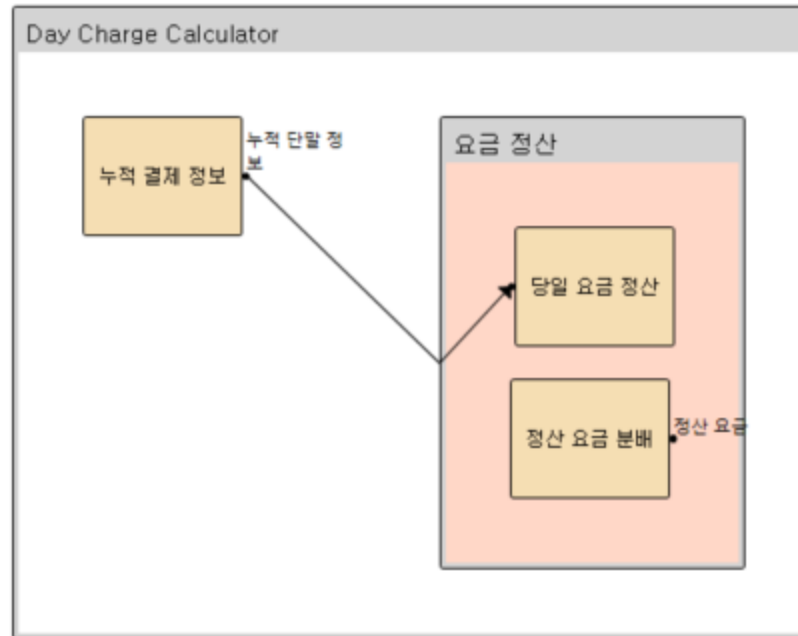
## - Logical Design Model



# RM+

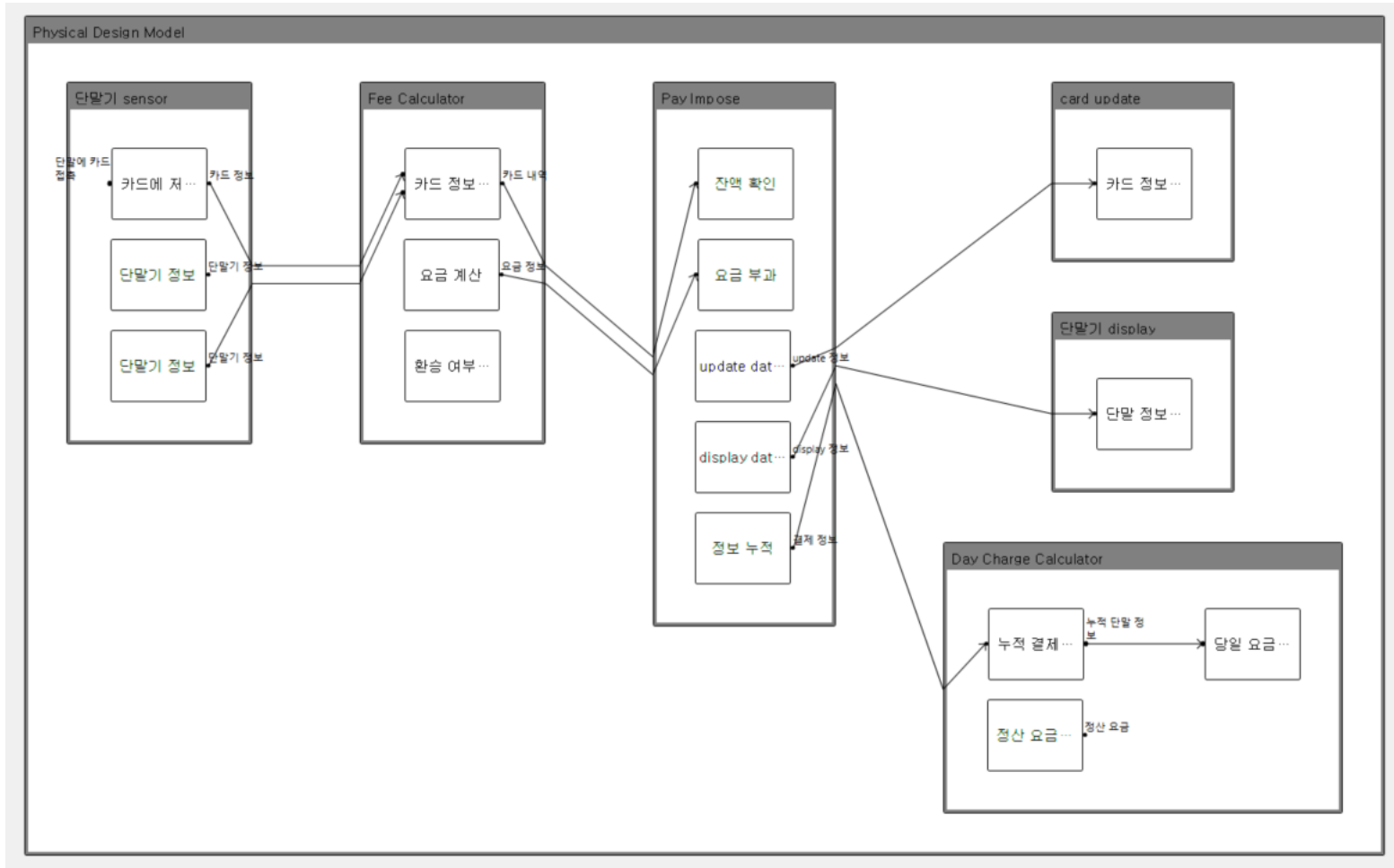
- Logical Design Model

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# RM+

## - Physical Design Model



Q & A

**END**