A Tool for Checking ANSI-C Programs

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Abstract

We present a tool for the formal verification of ANSI-C programs using Bounded Model Checking (BMC). The emphasis is on usability: the tool supports almost all ANSI-C language features, including pointer constructs, dynamic memory allocation, recursion, and the float and double data types. From the perspective of the user, the verification is highly automated: the only input required is the BMC bound. The tool is integrated into a graphical user interface. This is essential for presenting long counterexample traces: the tool allows stepping through the trace in the same way a debugger allows stepping through a program.

Contents

- 1. Introduction
- 2. Bounded Model Checking for ANSI-C Programs
- 3. A Graphical User Interface
- 4. Conclusion and Future Work

ANSI-C Language Features CBMC

- We present a tool that uses Bounded Model Checking to reason about low-level ANSI-C programs.
- There are two applications of the tool:

1) the tool checks safety properties such as the correctness of pointer constructs

2) the tool can compare an ANSI-C program with another design, such as a circuit given in Verilog.

- We describe a tool (CBMC) that formally verifies ANSI-C programs.
 - Checked include pointer safety, array bounds, and user-provided assertions.
 - Implements a technique called Bounded Model Checking (BMC) [1].
 - + GUI
- In BMC,
 - the transition relation for a complex state machine and its specification are jointly unwound to obtain a Boolean formula that is satisfiable if there exists an error trace.
 - The formula is then checked by using a SAT procedure.
 - If the formula is satisfiable, a counterexample is extracted from the output of the SAT procedure.
- The tool (CBMC) checks that sufficient unwinding is done to ensure that no longer counterexample can exist by means of *unwinding assertions*.

- Hardware Verification using ANSI-C as a Reference
- There are two implementations of the same design:
 (1) One written in ANSIC, which is written for simulation,
 (2) One written in register transfer level HDL, which is the actual product.
- The ANSI-C implementation is usually thoroughly tested and debugged. After testing and debugging the program, the actual hardware design is written using hardware description languages like Verilog. The Verilog description is then synthesized into a circuit.
- Due to market constraints,
- <u>An automated, or nearly automated way of establishing the consistency</u> of the HDL implementation with respect to the ANSI-C model is highly <u>desirable</u>.

- This motivates the verification problem: we want to verify the consistency
- of the HDL implementation, i.e., the product, using the ANSI-C implementation as a reference [2].
 - Establishing the consistency does not require a formal specification.
 - However, formal methods to verify either the hardware or software design are still desirable.
- The previous work focuses on a small subset of ANSI-C that is particularly close to register transfer language.
 - Thus, the designer is often required to rewrite the C program manually in order to comply with these constraints.
- Our tool supports the full set of ANSI-C language features.
- In order to verify the consistency of the two implementations, we unwind both the C program and the circuit in tandem.

2. Bounded Model Checking for ANSI-C Programs

- We reduce the Model Checking Problem to determining the validity of a bit vector equation.
- The process has five steps:
 - 1. We assume that the ANSI-C program is already preprocessed, e.g., all the #define directives are expanded.
 - 2. The loop constructs are unwound using assertions.
 - 3. Backward goto statements are unwound in a manner similar to while loops.
 - 4. Function calls are expanded.
 - 5. The program is then transformed into static single assignment (SSA) form, which requires a pointer analysis.

2.1 Generating the Formula

- The procedure above produces two bit-vector equations: *C (for the constraints)* and *P (for the property).*
- In order to check the property, we convert C ∧ ¬P into CNF by adding intermediate variables and pass it to a SAT solver such as Chaff [5].
 - If the equation is satisfiable, we found a violation of the property.
 - If it is unsatisfiable, the property holds.



2.2 Converting the Formula to CNF

- The conversion of most operators into CNF is straight-forward, and resembles the generation of appropriate arithmetic circuits.
- The tool can also output the bit-vector equation before it is flattened down to CNF, for the benefit of circuit level SAT solvers.

3. A Graphical User Interface

- To increase the usability of our tool, we have designed a user interface meant to be more familiar.
- The tool has two main possible applications:
 - Verification of properties of C programs
 - Checking consistency of Verilog designs against a C implementation
- When a counterexample is generated, the line number reported by CBMC is usually not pointing to the line that contains the actual bug.
- A version of CBMC modified by Alex Groce addresses the problem of error localization [6]: the tool displays which statements or input values are important for the fact that the property is violated.

4. Conclusion and Future Work

- We described a tool that formally verifies ANSI-C programs using Bounded Model Checking (BMC).
- The tool supports all ANSI-C operators and pointer constructs allowed by the ANSI-C standard, including dynamic memory allocation, pointer arithmetic, and pointer type casts.
- The user interface is meant to appeal to system designers, software engineers, programmers and hardware designers, offering an interface that resembles the interface of tools that the users are familiar with.

ANSI-C Language Features

Table 1.	Supported	language	features	and	implicit	properties
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Supporte	ed Language Features	Properties checked
Basic Data Types	All scalar data types float and double using fixed- point arithmetic. The bit-width can be adjusted using a com- mand line option.	
Integer Operators	All integer operators, including division and bit-wise operators Only the basic floating-point operators	Division by zero Overflow for signed data types
Type casts	All type casts, including con- version between integer and floating-point types	Overflow for signed data types
Side effects	CBMC allows all compound oper- ators	Side effects are checked not to affect variables that are evalu- ated elsewhere, and thus, that the ordering of evaluation does not affect the result.
Function calls	Supported by inlining. The lo- cality of parameters and non- static local variables is pre- served.	 Unwinding bound for recur- sive functions Functions with a non-void return type must return a value by means of the re- turn statement.
Control flow statements	<pre>goto, return, break, continue, switch ("fall-through" is not supported)</pre>	
Non-Determinism	User-input is modeled by means of non-deterministic choice functions	
Assumptions and Assertions	Only standard ANSI-C expres- sions are allowed as assertions.	Assertions are verified to be true for all possible non- deterministic choices given that any assumption executed prior to the assertion is true.
Arrays	Multi-dimensional arrays and dynamically-sized arrays are supported	Lower and upper bound of ar- rays, even for arrays with dy- namic size

Table 2. Supported language features and implicit properties

Support	ed Language Features	Properties checked
Structures	Arbitrary, nested structure types; may be recursive by means of pointers; incom- plete arrays as last element of structure are allowed	
Unions	Support for named unions, anonymous union members are currently not supported	CBMC checks that unions are not used for type conversion, i.e., that the member used for read- ing is the same as used for writ- ing last time.
Pointers	Dereferencing	When a pointer is dereferenced, CBMC checks that the object pointed to is still alive and of matching type. If the object is an array, the array bounds are checked.
	Pointer arithmetic	
	Relational operators on pointers	CBMC checks that the two operands point to the same object.
	Pointer Type Casts	Upon dereferencing, the type of the object and the expression are checked to match
	Pointers to Functions	The offset within the object is checked to be zero
Dynamic Memory	malloc and free are supported. The argument of malloc may be a nondeterministically cho- sen, arbitrarily large value.	Upon dereferencing, the object pointed to must still be alive. The pointer passed to free is checked to point to an object that is still alive. CBMC can check that all dynamically allocated memory is deallocated before exiting the program ("memory leaks").

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Fig. 1. The tool is able to automatically check the bound selected by the user for the unwinding of loops. If the given bound is not sufficient, the tool suggests to provide a larger bound.

🗷 cbmcUl - [MicroC/OS SemPe	nd]		
File Project Trace Help			
microos.c			
assert (LOCK != 0);			
LOCK = 0;			
1			
void OSSemPend(OS_EV	ENT *pevent , INT16U time	sout , INT6U *err)	-
1			
assume (LOCK == 0);			
			<u> </u>
Sources Traces Error Outrat	Debug 1		
Solving with 2Chaff version 2Chaff 200	3.6.16		~
3017 variables, 822 clauses	EADLE in domand hold		-
assertion	TABLE, I.e., does not hold		
Verfication failed			
<u></u>			<u> </u>
Name	Value		
LOCK		000000000000000000000000000000000000000	
OSEventTO::pevent	INVALID		
OSEventTaskWait:pevent	INVALID		
OSIntNesting	1 (00000001)		
OSSemPend::pevent	INVALID		
timeout	0 (000000000000000000000000000000000000	000000000000000000000000000000000000000	
	MicroC/OS SemPend	Lock Error: 12 of 12	assertion

Fig. 2. The Watches windows allows keeping track of the current values of the program variables. In this case, the assertion failed because the variable LOCK has value 0.

lle Project Trace Help					Chemical Che
ps2 kayboard.c ps2_keyboard.v					
Nonjusaus Encoded Nonjusaus Encoded	hich I considered importat dd the appropriate case s the keyboard scan codes a n ascending order of ASC de = (3*0.rx_shift_key_o _code) 8. // Backspace (*backspace) 9. // Horizontal Tab d; // Carriage return (*ent b; // Escape (*esc**key) 0. // Space Debug Result	nt have been included. tatement lines you wish to assign.] value. nn.q[8:1]]; ace" key] of" key]			
Missing Include File Erro	rs				
Array Bounds Faile	ed: array upper bound				
Signal	Û	1	2	3	4
Signal ascii	0 (0 (0000000)	1	2	3	4
Signal ascii bit_count	0 (0_0000000) (0_00000)	1	2	3	4
Signal ascii bit_count clk	0 0 (0000000) 0 (0000)	1	2	3	4
Signal ascii bit_count clk enable_timer_Susec	0 0 (0000000) 0 (0000)	1	2	3	4
Signal ascii bit_count clk enable_timer_Susec enable_timer_60usec	0 0 (0000000) 0 (0000)	1	2	3	4
Signal ascii bit_count cik enable_timer_5usec enable_timer_60usec hold_extended	0 0 (0000000) 0 (0000)	1	2	3	4
Signal ascii bit_count cik enable_timer_5usec enable_timer_60usec hold_extended hold_released	0 0 (0000000) 0 (0000)	1	2	3	4
Signal ascii bit_count cik enable_timer_Susec enable_timer_SOusec hold_extended hold_released left_shift_key	0 0 (0000000) 0 (0000)		2	3	4
Signal ascii bli_count clk enable_timer_Susec enable_timer_SUsec hold_extended hold_released left_shift_key m1_next_state	0 0 (000000) 0 (0000)	1 13 (1101)	2	3 (1 (0001) (14 (1110))	
Signal ascii bit_count clk enable_timer_5usec enable_timer_60usec hold_extended hold_released left_shit_key m1_next_state var::m1_state	0 0 (000000) 0 (0000) 	1 	2 0 (0000) 13 (1101)	3 (1 (0001) () () () (4
Signal ascii bit_count clk enable_timer_Susec enable_timer_Susec hold_extended hold_released left_shit_key m1_next_state var::m1_state m2_next_state	0 0 (0000000) 0 (00000) 	1 (2	3 (1 (0001) (4
Signal ascii bit_count clk enable_timer_Susec enable_timer_Susec hold_extended hold_released left_shift_key m1_next_state war:m1_state m2_next_state m2_state	0 0 (0000000) 0 (00000) 	1 	2	3 (1 (0001) (4
Signal ascii bit_count clk enable_timer_5usec enable_timer_60usec hold_extended hold_released left_shift_key m1_next_state var::m1_state m2_next_state m2_state var::ps2_clk	0 0 (0000000) 0 (0000) 0 (0000) 0 (0000) 0 (0000) 0 (0000)	1 	2	3 (1 (0001) (4
Signal ascii bit_count clk enable_timer_Susec enable_timer_Susec hold_extended hold_released left_shift_key m1_next_state war::m1_state m2_next_state war::ps2_clk ps2_clk_bi_z		1 	2	3 (1 [0001] (
Signal ascii bit_count clk enable_timer_Susec enable_timer_Susec hold_extended hold_released left_shift_kcy ml_next_state var::ml_state m2_next_state var::ps2_clk ps2_clk_bi_z ps2_clk_s		1 <u>13 (1101)</u> <u>1 (0001)</u>	2 0 [0000] 13 [1101]	3 (1 (0001) (

Fig. 3. The Signals window shows the values of the variables in a Verilog design using a waveform representation.



Fig. 4. The Project Options dialog allows setting up the parameters.