# embedded software.....

# Formal Modeling and Verification of Safety-Critical Software

Junbeom Yoo, Konkuk University Eunkyoung Jee, Korea Advanced Institute of Science and Technology Sungdeok Cha, Korea University

A formal-methodsbased process for developing safety-critical software supports development, verification and validation, and safety analysis and has proven to be effective and easy to apply. igorous quality demonstration is important when developing safety-critical software such as a nuclear power plant's reactor protection system (RPS). Although stakeholders strongly recommend using formal modeling and verification, domain experts often reject such methods because the candidate techniques are overabundant, the notations appear complex, the tools often work only in isolation, and the output is frequently too difficult for domain experts to understand and to extract meaningful information.

To overcome such obstacles, we developed a formal-methods-based process that supports development, verification, and safety analysis. We also developed CASE tools to let nuclear engineers apply formal methods without having to know the underlying formalism in depth. In this article, we describe more than seven years' experience working with nuclear engineers in developing RPS software and applying formal methods. Nuclear engineers and regulatory personnel found the process effective and easy to apply with our integrated tool support.

## Developing a Digital Control System

When developing and verifying safety-critical software, formal methods are important for increasing safety assurance and demonstrating compliance with strict regulations. In 2001, the Korean Nuclear Instrumentation and Control System consortium (KNICS; www.knics.re.kr) began developing a digital control system for the APR-1400 reactor. At the project's start, project managers made two decisions that strongly influenced our process:

- When developing safety-critical components such as an RPS, we would use formal methods whenever it was practical to do so.
- Software development would be based on the programmable logic controller (PLC), using function block diagram (FBD) as the implementation language.

As a software engineering research group in computer science, we began working with nuclear engineers to produce a formal requirements specification, develop necessary CASE tools, and conduct formal verification during software development. Figure 1 describes the overall process we developed, which covers three essential aspects of safety-critical software: development, formal verification, and safety demonstration.



Our group developed the CASE tools marked with an asterisk in the figure.

Although the process is similar to that of a typical software project, little development activity occurs beyond the design phase. Once the final FBD design has successfully completed safety analysis and verification and has been officially approved, a compiler provided by the PLC vendor automatically generates executable code. So, it's fair to treat an FBD as an implementation language, too. Also, a different group tested the software extensively at various levels, according to the standard practices.

In developing the formal-methods-based process in Figure 1, we insisted on three core principles. First, we tried to honor the end users' and stakeholders' opinions whenever practical. In our project, nuclear engineers developing a plant instrumentation and control system were the most important user group. The government's regulatory personnel were also important stakeholders. They needed to review and approve all software requirements, designs, and associated documents for the system to be certified for operation. Because the regulatory agency had experience reviewing a similar system (currently used in a Wolsung plant in Korea), many of the project personnel were familiar with software cost reduction (SCR) and SCR-like tabular notations.<sup>1</sup> However, they felt uneasy about exclusively using the tabular notations. So, we chose the syntax of Nu-SCR,<sup>2</sup> an SCR-like formal specification language that we customized for nuclear applications, to address the domain experts' concerns. We chose to retain tabular notations with relaxed rules on expressions while introducing automata-like notations for specifying timing behavior. Once the notations became fixed, we defined formal semantics so that we could perform automated analysis and develop the CASE tool. Choosing notations that the domain experts will accept is the first step toward successfully applying formal methods in industrial environments.

Second, we were determined not to reinvent the wheel, by using techniques and tools already proven effective. For example, model-checking theory and tools are mature enough, and we wanted seamless integration with our process. Because FBD was our implementation language, we chose model checkers that would work well with it. For example, because we expected the initial Figure I. Software development, verification, and safety analysis for the Korean Nuclear Instrumentation and Control System (KNICS) consortium's reactor protection system software. CASE tools marked with an asterisk were developed by the authors.



#### Figure 2. NuSRS 2.0: A CASE tool for

2.0: A CASE tool for NuSCR specification and verification. The formal modeling and verification tool significantly improves software development productivity as well as safety assurance because it can detect many errors early and automatically. FBD design to go through multiple revisions and releases, we were interested in an equivalence verification feature of the VIS (Verification Interacting with Synthesis; http://embedded.eecs.berkeley. edu/research/vis) model checker. Another important factor was a relatively small semantic gap between FBD and Verilog. Because the VIS and Cadence SMV (Symbolic Model Verifier; www. kenmcmil.com/smv.html) model checkers can process Verilog as their inputs, we developed FBD-to-Verilog translation rules and proved semantic equivalence to utilize Cadence SMV and VIS. It's essential to choose "industrial strength" formal methods proven effective in similar applications rather than preaching the pet formalism of formal-method experts.<sup>3</sup>

Third, we provided proper tool support to make formal methods as easy and intuitive as possible. Although VIS equivalence checking was apparently highly useful, nuclear engineers couldn't accept a text-based tool interface. It's nearly impossible for them to understand the output or understand why two designs behave differently. The nuclear engineers didn't have the time for or interest in learning VIS technical details to investigate why two designs revealed different behavior after seven states. Formal-method experts shouldn't blame nuclear engineers for this attitude. Likewise, understanding a Cadence SMV counterexample is really daunting to most people who aren't formalmethods experts. To bridge such semantic gaps, we developed visualization tools so that domain experts could focus on semantic analysis in familiar notations without being overwhelmed by low-level, often partial, and sometimes redundant raw data. For formal methods to be successfully applied in industry, there must be a reasonable interpretation of the results using the terms domain experts understand. Visualization is often the most effective approach.

### **Development**

To begin requirements analysis, the domain experts prepared a natural-language specification, and we worked with nuclear engineers to prepare formal specification in NuSCR. NuSCR refers to a specification language and the approach we developed, not a document. Hands-on tutorial sessions helped them better understand NuSCR's syntax and semantics. As the language was defined-in close consultation with an expert who understood both domains-most developers accepted NuSCR without much difficulty or resistance. However, at their request, we relaxed rules on expressions on structured decision tables (SDTs), compared to the SCR method, in that NuSCR allowed relational and range expressions. Domain experts insisted that those equations they would be forced

to break into multiple subexpressions actually represent accurate "atomic" domain knowledge, and that automated analysis of completeness and consistency is unnecessary. However, they had trouble understanding specification of timing-related behavior in tabular notation, and they clearly preferred automata-like diagrams.

Our group worked with domain experts in developing a formal specification for two of the four major subsystems, whose natural-language specification was nearly 200 pages long. We developed the formal specification in NuSCR notation, following a process similar to the one Nancy Leveson and her graduate students used to develop a formal specification for the TCAS (Traffic Alert and Collision Avoidance System) for aviation.<sup>4</sup> Nearly 200 NuSCR nodes (for example, SDTs and automata) were scattered in nearly 20 group nodes organized hierarchically. We used the NuSRS CASE tool we developed (see Figure 2).

NuSCR uses a finite-state machine (FSM) to specify state-dependent operations and a timed transition system (TTS), a variant of automata, to specify timing-related requirements. We made various nodes different shapes and colors so that we could easily see their roles. Naming conventions (such as  $f_{-}$  for functions,  $b_{-}$  for history variables, and  $th_{-}$  for timed history variables) also indicate the role. In addition, the function overview diagram (see the middle of Figure 2) illustrates which NuSCR nodes are included in a group node whose prefix is g\_. Furthermore, all the externally visible inputs and outputs are organized in groups and shown on the left along with their attributes. NuSRS 2.0 supports XML-based interfaces and includes menus to perform automated translation to inputs accepted by Cadence SMV.

Once the domain experts understood NuSCR notation and a reasonably stable CASE tool became available, nuclear engineers could specify most of the formal specification (although they needed our help occasionally). During requirements analysis, domain experts inspected the NuSCR models. Our research group also used Cadence SMV to see whether the NuSCR specification preserved required properties.

Once the experts approved and baselined the formal specification in NuSCR, we could synthesize semantically equivalent FBD designs using rules from our previous research.<sup>5</sup> We emphasized semantic-preserving and correct synthesis rather than an optimal generated FBD design. For example, when some expressions appeared several times in the specification, the synthesized FBD



#### **Figure 3. NuSCRtoFBD:**

contained redundancy although it was semantically correct. Our experiment revealed that synthesized FBD programs often contain more than twice the number of FBD blocks than manually coded and optimized designs. In the nuclear application, correctness and safety are the most important quality criteria because regulator personnel must rigorously review the design. In addition, there are only a few installations at most, and cost saving through optimal design is rarely a practical concern. However, in different application domains (automotive control systems in particular), an optimal design would become a critical requirement owing to the sheer number of systems to be produced in a highly competitive market.

Synthesized design is a useful starting point for engineers to revise and develop official FBD design. Many FBD engineers felt that manual FBD programming, regardless of the specification notations used, was the most error-prone activity. Unfortunately, we couldn't use our FBD synthesis tool, NuSCRtoFBD (see Figure 3), because our team couldn't develop all the necessary CASE tools in time. However, when we consulted the nuclear engineers after the tool development, they felt that such a tool would have significantly improved their productivity.

#### Verification

For safety-critical software such as RPS, engineers must perform verification after each phase.<sup>6</sup> Although inspecting the requirements document and FBD design is useful, it's insufficient for meeting rigorous regulatory requirements. During requirements analysis, we developed rules to translate the NuSCR specification into language the Cadence SMV model checker could accept. We implemented automatic translation and seamless A CASE tool for automatic FBD synthesis from NuSCR. Integrated support for formal methods is critical. If one is forced to manually develop an FBD design from a formal specification, such an approach is unlikely to win acceptance in industry.

			74 FIX_RISING.v					
Relvant to CE	Verilog CE from P2	0	<u>File Prop View G</u> ot	o History	Abstra	ction		Help
# Part of FIX_RISING	CI-0 ヴ 구18-Framework-IEEE software-jbyool/FBDVerifier例 別/FD/、RISING.v			i i	1	i i	_	
// (Incomplete ST)	module main (clk, HYS, MAXCNT, PHYS, PV_OUT);		<u>B</u> rowser Properties	<u>R</u> esult	s <u>C</u> one	Usi <u>ng</u>	Groups	
TRIP_CNT_out :=	input clk; input [2:0] HYS;		All results	+				
G :=	input [4:0] MAXCNT;			<u> </u>				
AND ( = 101 = 1000 = 100 = 100 = 100 = 100 = 100 = 100 = 100 = 100 = 100 = 100	reg [4:0] PTRIP_CNT;		Property Result		Ti	me		
GE (	reg PTRIP_LOGIC; reg [7:0] PTSP;		P1 true S	Sat Dec 27 1	7:30:42 ëg	<ul><li>圖誘 월 명 (응</li></ul>	봀以 i얚 2008	
PV_OUT,	input [7:0] PV_OUT;		P2 false S	Sat Dec 27-1	7:30:43 ēg	·圖誘꼴빙 ()	影以 i뫢 2008	
TSP),	reg TRIP_LOGIC;							
IN2 := NOT TRIP_LOGIC)	Leg [//0] 13F,		Source Trace Loo	1				
IN0 :=	wire [5:0] PTRIP_CNT_out; wire PTRIP LOGIC 1;		Torne   Trace   Tos	,				
IN1 :=	wire [7:0] PTSP 1;		File Edit Run Viev	N				
ADD ( IN1 :=	wire TRIP_LOGIC_1;			-		_	_	
TRIP_CNT, IN2 :=	wire TRIP_LOGIC_out;		1	2	3	4	5	6
1))	wire [8:0] TSP_out; wire PTRIP LOGIC out;		PV_OUT[0] 0	0	0	0	0	0
TRIP_LOGIC_1 :=	wire [8:0] PTSP_out;		PV_OUT[1] 0	0	0	0	0	0
SEL( G ;=	//constants		PV_0UT[2] 0	0	0	0	0	0
GE ( IN1 :=	assign MAXCNT = 10;		PV_0UT[3] 0	0	0	0	0	0
TRIP_CNT_out,	assign PHYS = 1;		PV_OUT[4] 0	0	0	0	0	0
MAXCNT),	initial begin	1	PV OUT[5] 0	0	0	0	0	0
TRIP_LOGIC,			PV OUTI61 0	0	0	0	0	0
MV ended with code 0			PV OUTIZI 1	1	1	1	1	1
a)		- 1	TRIP_CNTI01_0	1	0	1	0	1
aj			TRIP_CNT[1] 0	0	1	1	0	0
				0	-	-	1	1
				0	0	0	1	1
				0	0	0	0	0
FBD Verifier	e' e' 🛛			1.0				
FBD Verifier ile Verify Help	a a a		TRIP_CNT[4] 0	0	0	0	0	0
FBD Verifier ile Verify Help PLC Retvant to Fart of FIX_RISING	o"o"⊠ verskog CEfrom P2 Displaying verskake: Input Ø Reg ⊘Output Ø		TRIP_CNT[4] 0 TRIP_CNT_out[0] 1	0	0	0	0	0
FBD Verifier       ile     Verifiy       Help       Plc     Relvant tr       Part of FIX_RISING       f (incomplete ST)	o"o" ⊠ Verskog CE from P2 Displaying versikke: Input ℤ Reg ℤ Output ℤ Original CE Reduced form Timing graph Sliced vars Warnings		TRIP_CNT[4] 0 TRIP_CNT_out[0] 1 TRIP_CNT_out[1] 0	0 0 1	0 1 1	0 0 0	0 1 0	0 0 0 1
FBD Verify Help      PLC     Relvant t     FPLC     Relvant t     (     rest of FDX_RISING     (     Incomplete ST)      IRIP_TIMER_IN =     AND (	ro ro 2 Prestavleng vortable: Input 2 Reg ≥ Output 2 Original CE: Reduced form Timing graph Sliced vars Warnings		TRIP_CNT[4]         0           TRIP_CNT_out[0]         1           TRIP_CNT_out[1]         0           TRIP_CNT_out[2]         0	0 0 1 0	0 1 1 0	0 0 0 1	0 1 0 1	0 0 1 1
FBD Verifier  ile Verify Help  PLC Relvant to  PArt of FbC_RISING  (ncomplete ST)  RRIP_TIMER_IN = AND ( INT = 0E (	o 'a' ⊠ Dispanjong veriable: Input ⊘ Reg ⊘ Output ⊘ Original CE Produced farm Timing graph Sliced vars Warnings Vortunt SP Vortunt TSP		TRIP_CNT[4]         0           TRIP_CNT_out[0]         1           TRIP_CNT_out[1]         0           TRIP_CNT_out[2]         0           TRIP_CNT_out[3]         0	0 0 1 0 0	0 1 1 0 0	0 0 0 1 0	0 1 0 1 0	0 0 1 1 0
FBD Verifier           ile Verify Help           DPLC Revent to PLC Revent to Complete ST)           IRIP_TIMER_IN = AND (INT = OE (INT = PV OIT)	Warking         CE from P2           Displays writikke:         Input Ø Reg Ø Urlput Ø           Orlightal CE         Reduced farm           Trings graph         Staced vars           Warkings         P           PV_OUT         Staced vars           Warkings         P           PR         0           0         0           0         0           0         0           0         0           0         0           0         0           0         0           0         0           0         0           0         0		TRIP_CNT[4] 0 TRIP_CNT_out[0] 1 TRIP_CNT_out[1] 0 TRIP_CNT_out[2] 0 TRIP_CNT_out[3] 0 TRIP_CNT_out[4] 0	0 0 1 0 0 0	0 1 1 0 0 0	0 0 1 0 0	0 1 0 1 0 0 0	0 0 1 1 0 0
TBO Ventifier           Bite Ventify Help           [Pace] Research	v Versing CE from P2 Displaying writikke: Input ≥ Reg ≥ Output ≥ Original CE: Reduced form Timing graph Skicel vars Warnings PV_OUT TSP P6 00 50 50 50 50 50 50 50 50 50 50 50 50		TRIP_CNT[4]         O           TRIP_CNT_out[0]         1           TRIP_CNT_out[1]         0           TRIP_CNT_out[2]         0           TRIP_CNT_out[3]         0           TRIP_CNT_out[4]         0           TRIP_CNT_out[4]         0	0 0 1 0 0 0 0	0 1 1 0 0 0 0 0	0 0 0 1 0 0 0	0 1 0 1 0 0 0 0	0 0 1 1 0 0 0
FBO Ventifier           Be Venty Help           PLC         Relvant K           PLT         Relvant K           (*) ▼ C	Warking         CE from P2           Original CE         Reg ≥ Output ≥           Original CE         Reduced form           PV_OUT         Image graph           Sked vars         Warnings           PAP_OUT         Image graph           Sked vars         Warnings           PAP_OUT         Image graph           Sked vars         Image graph           TRP_TMER_0         THUP_LOG/C		TRIP_CNT[4]           TRIP_CNT_out[0]           TRIP_CNT_out[1]           TRIP_CNT_out[2]           TRIP_CNT_out[3]           TRIP_CNT_out[4]           TRIP_LOGIC           TRIP_LOGIC	0 0 1 0 0 0 0 0 0	0 1 1 0 0 0 0 0 0	0 0 1 0 0 0 0 0	0 1 0 1 0 0 0 0 0	0 0 1 1 0 0 0 0 0 0
IBO Ventifier           Be Venty Help           IPLC         Relvant ft           IPLC         Relvant ft           IPLC         Relvant ft           IPL         Relvant ft	Warking         CE from P2           Original GE         Reg ≥ Output ≥           Original GE         Reduced form           Traip         100           TRP_LOGC         10           Traip         100		TRIP_CNT[4]           TRIP_CNT_out[0]           TRIP_CNT_out[1]           TRIP_CNT_out[2]           TRIP_CNT_out[3]           TRIP_CNT_out[4]           TRIP_LOGIC           TRIP_LOGIC_1           TRIP_LOGIC_out	0 0 1 0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0 0	0 0 1 0 0 0 0 0 0 0	0 1 0 1 0 0 0 0 0 0 0	0 0 1 1 0 0 0 0 0 0 0 0 0
IBD Ventity Holp           ■ Part of Park of	Warking         CE from P2           Original CE         Reg ⊘ Output ⊘           Original CE         Reduced form           Train         Train           TRP_INER_N         TRP_INER_N		TRIP_CNT_out[0] 1 TRIP_CNT_out[0] 1 TRIP_CNT_out[1] 0 TRIP_CNT_out[2] 0 TRIP_CNT_out[3] 0 TRIP_CNT_out[4] 0 TRIP_LOGIC 0 TRIP_LOGIC 1 TRIP_LOGIC_0U 0 TRIP_LOGIC_1 1 TRIP_LOGIC_1 1 TRIP_LOGIC_1 1	0 0 1 0 0 0 0 0 0 0 1	0 1 1 0 0 0 0 0 0 0 0 1	0 0 1 0 0 0 0 0 0 0 1	0 1 0 1 0 0 0 0 0 0 0 1	0 0 1 1 0 0 0 0 0 0 1 1
IBD Working           ■ Verity Holp           ■ PLC         Reshard for the processing of the procesesing of the procesesing	Warding         CE from P2           Dispskywardiake:         Input I           Original CE         Reduced form           Wording         Things graph           Siliced vars         Warnings           Wording         Things graph           Siliced vars         Warnings           Wording         Things graph           Siliced vars         Warnings           Wording         Things graph           Warning         Things graph           Trap         Things graph		TRIP_CNT_out[0] 1 TRIP_CNT_out[0] 1 TRIP_CNT_out[1] 0 TRIP_CNT_out[2] 0 TRIP_CNT_out[3] 0 TRIP_CNT_out[4] 0 TRIP_LOGIC 0 TRIP_LOGIC 1 TRIP_LOGIC_1 0 TRIP_LOGIC_out 0 TSP[0] 1 TSP[1] 0	0 0 1 0 0 0 0 0 0 1 0	0 1 1 0 0 0 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 0 1 0	0 1 0 1 0 0 0 0 0 0 1 1 0	0 0 1 1 0 0 0 0 0 0 1 0
FBO Ventify           ■ Venty	Verting     CE from P2		TRIP_CNT[4]           TRIP_CNT_out[0]           TRIP_CNT_out[1]           TRIP_CNT_out[2]           TRIP_CNT_out[3]           TRIP_CNT_out[4]           TRIP_CNT_out[4]           TRIP_COGIC_0           TRIP_LOGIC_1           TRIP_LOGIC_out           TSP[0]           TSP[1]	0 0 1 0 0 0 0 0 0 1 0 0 0	0 1 1 0 0 0 0 0 0 1 1 0 0	0 0 1 0 0 0 0 0 0 1 1 0 0	0 1 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
IBD Working           ■ Verity Help           ■ LC         Relvent fr ■ ■ c           ■ PLC         Relvent fr ■ ■ c           0 PLC         Relvent fr ■ ■ c           0 Relvent fr = = Relvent fr         Relvent fr           0 Relvent fr         Relvent fr           0 Relvent fr         Relvent fr           0 Relvent fr         Relvent fr           N0 Train_LOOIC_1.out = SEL         SEL           0 Mo = Train         Relvent frame_LOOIC           N0 = Train         Relvent frame_LOOIC	Normality         CE from P2           Displays writikle:         Reg ⊘ Output ⊘           Original CE:         Reduced from           Displays writikle:         Image graph           Steed vars         Warnings           PV_OOT         Steed vars           Warning         Image graph           Steed vars         Warnings           PV_OOT         Steed vars           Warning         Image graph           Image graph         Image graph           Image graph         Image graph           PV_OOT         Steed vars           Variange         Image graph           Image graph         Image graph<		TRIP_CNT[4]         0           TRIP_CNT_out[0]         1           TRIP_CNT_out[1]         0           TRIP_CNT_out[2]         0           TRIP_CNT_out[3]         0           TRIP_CNT_out[4]         0           TRIP_CNC_out[4]         0           TRIP_LOGIC         0           TRIP_LOGIC_out         0           TSP[0]         1           TSP[1]         0           TSP[2]         0	0 0 1 0 0 0 0 0 0 0 1 0 0 1 1	0 1 1 0 0 0 0 0 0 1 1 0 0 1	0 0 1 0 0 0 0 0 0 1 0 0 1 0 0 1	0 1 0 1 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 0 0 0 0 0 0 1 1 0 0
IBD Winfler           ■ Verity Help           ■ PLC         Relvent fr(	Warding         CE from P2           Insight/mg writible:         Insight/mg w		TRIP_CNT[4]           TRIP_CNT_out[0]           TRIP_CNT_out[1]           TRIP_CNT_out[2]           TRIP_CNT_out[3]           TRIP_CNT_out[4]           TRIP_CNT_out[4]           TRIP_LOGIC           TRIP_LOGIC_0           TRIP_LOGIC_out           TSP[0]           TSP[0]           TSP[2]           TSP[3]           TSP[3]	0 0 1 0 0 0 0 0 0 0 1 0 0 1 1 1	0 1 1 0 0 0 0 0 0 0 1 0 0 1 1 1 1	0 0 0 1 0 0 0 0 0 1 1 0 0 1 1	0 1 0 1 0 0 0 0 0 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 0 0 0 0 0 1 1 1 1
H0 VentWer	P         Original CE: from P2           Displaying writikke: Input IP         Reg IP Output IP           Original CE: Reduced form         Timing graph           Skied vars         Warnings           PV_OUT         IP           P8         00 <t< td=""><td></td><td>TRIP_CNT[4]         0           TRIP_CNT_out[0]         1           TRIP_CNT_out[1]         0           TRIP_CNT_out[2]         0           TRIP_CNT_out[3]         0           TRIP_CNT_out[4]         0           TRIP_LOGIC         0           TRIP_LOGIC_1         0           TRIP_LOGIC_0ut         0           TSP[0]         1           TSP[1]         0           TSP[2]         0           TSP[3]         1           TSP[4]         0</td><td>0 0 1 0 0 0 0 0 0 1 0 0 1 1 0 0</td><td>0 1 1 0 0 0 0 0 0 1 1 0 0 1 1 1 0</td><td>0 0 1 0 0 0 0 0 0 1 1 0 0 1 1 1 0</td><td>0 1 0 1 0 0 0 0 0 1 1 0 1 1 0 1 1 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td>0 0 1 1 0 0 0 0 0 1 0 0 1 1 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0</td></t<>		TRIP_CNT[4]         0           TRIP_CNT_out[0]         1           TRIP_CNT_out[1]         0           TRIP_CNT_out[2]         0           TRIP_CNT_out[3]         0           TRIP_CNT_out[4]         0           TRIP_LOGIC         0           TRIP_LOGIC_1         0           TRIP_LOGIC_0ut         0           TSP[0]         1           TSP[1]         0           TSP[2]         0           TSP[3]         1           TSP[4]         0	0 0 1 0 0 0 0 0 0 1 0 0 1 1 0 0	0 1 1 0 0 0 0 0 0 1 1 0 0 1 1 1 0	0 0 1 0 0 0 0 0 0 1 1 0 0 1 1 1 0	0 1 0 1 0 0 0 0 0 1 1 0 1 1 0 1 1 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 0 0 0 0 0 1 0 0 1 1 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
TBD Ventitive           ■ Verity Holp           ■ PLC         Relxhaut (           ■ Relxhaut (         ■ ■           ■ ■         ■           ■ ■         ■           ■ ■         ■           ■ ■         ■           ■ ■         ■           ■ ■         ■           ■ ■         ■           ■ ■         ■           ■         ■           ■         ■           ■         ■           ■         ■           ■         ■           ■         ■           ■         ■           ■         ■           ■         ■           ■         ■	Displayer with Michael P2 Displayer with Michael P2 Displayer with Michael P2 Displayer with Michael P2 Displayer P2 Displ		TRIP_CNT_out[0] 1 TRIP_CNT_out[0] 1 TRIP_CNT_out[0] 1 TRIP_CNT_out[1] 0 TRIP_CNT_out[2] 0 TRIP_CNT_out[4] 0 TRIP_LOGIC_1 0 TRIP_LOGIC_1 0 TRIP_LOGIC_0ut 0 TRIP_LOGIC_out 0 TSP[0] 1 TSP[1] 0 TSP[2] 0 TSP[3] 1 TSP[4] 1 TSP[5] 0 TSP[5] 1	0 0 1 0 0 0 0 0 0 1 1 0 0 1 1 0 0	0 1 1 0 0 0 0 0 1 0 1 1 0 1 1 0 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 1 0 0 0 0 0 1 0 0 1 0 0 1 0 0 1 0 0 0 1 0 0 0 0 1 0	0 1 0 1 0 0 0 0 0 1 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 0 0 0 0 0 0 1 1 0 0 1 1 0 0
TBD VentWer           ■ Venty Holp           ■ PLC         Renkent f(	Normalize         Control IS           Produced form         Training graph         Sided vars         Warning           Produced form         Sided vars         Warning         Sided vars         Sided vars           Produced form         Sided vars         Sided vars         Warning         Sided vars         Sided vars           Produced form         Sided vars         Sided vars         Sided vars         Sided vars         Sided vars           Produced form         Sided vars         Sided vars         Sided vars         Sided vars         Sided vars           Produced form         Sided vars         Sided vars         Sided vars         Sided vars         Sided vars           TRIP_INGR_IN         Sided vars         Sided vars         Sided vars         Sided vars         Sided vars         Sided vars           TRIP_INGR_IN         Sided vars         Sided vars         Sided vars         Sided vars         Sided vars         Sided vars           TSP_INGR_IN         Sided vars         S		TRIP_CNT[4]         0           TRIP_CNT_out[0]         1           TRIP_CNT_out[1]         0           TRIP_CNT_out[2]         0           TRIP_CNT_out[3]         0           TRIP_CNT_out[4]         0           TRIP_CNT_out[4]         0           TRIP_LOGIC         0           TRIP_LOGIC_1         0           TSP[0]         1           TSP[1]         0           TSP[2]         0           TSP[2]         0           TSP[2]         0           TSP[2]         0           TSP[2]         0           TSP[4]         1           TSP[5]         0           TSP[6]         0           TSP[6]         0	0 0 1 0 0 0 0 0 0 0 1 1 0 0 1 1 0 1 1 0 0	0 1 1 0 0 0 0 0 1 0 1 1 0 1 1 0 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0 0 1 0 0 1 1 1 0 0 1 1 1 0	0 1 0 1 0 0 0 0 1 0 0 1 1 1 0 1 1 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 0 0 0 0 1 1 1 1 0 0 1 1 0 0 1 1 0 0 0 1 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
IBD Winther           ■ Verity Help           ■ Let Verity Help           ■ Let Verity Help           ■ Part of FLC, FISINO           (monomplet ST)           ■ RPP_TMERE_IN >=           AND (           INI =           0 E (           INI >           FV_OUT,           IN2 =           TSP,           NOT TRIP_LOOIC)           NOT TRIP_LOOIC,           NOT REP_LOOIC,           IN0 =           10           TSP,           TRP_TMER_Q,           INI =           10           TSP,           TRP_TMER_Q,           IN1 =           SEL (           0 =           10           TSP,           TSP,           ND =           IN =           SUB (	Normality         CE from P2           Displayed writikke:         Reg ⊘ Output ⊘           Original CE         Reduced farm           Displayed farm         B           PV_OOT         TSP           PV_OOT         B           PP_LOGIC         Imming graph           Silcel vars         Warning           PV_OOT         TSP           P0         0           0         0           0         0           178P_LOGIC         Imming graph           TRP_TINER_N         THIP_LOGIC           TRP_TINER_N         Imming graph           TSP_for         Imming graph           TSP_for </td <td></td> <td>TRIP_CNT[4]           TRIP_CNT_out[0]           TRIP_CNT_out[1]           TRIP_CNT_out[2]           TRIP_CNT_out[3]           TRIP_CNT_out[4]           TRIP_CNT_out[4]           TRIP_CNT_out[4]           TRIP_COGIC_1           TRIP_LOGIC_0           TSP[0]           TSP[0]           TSP[2]           O           TSP[2]           TSP[3]           TSP[4]           TSP[5]           TSP[6]           TSP[7]</td> <td>0 0 1 0 0 0 0 0 0 0 1 0 0 1 1 0 1 0 1 0</td> <td>0 1 1 0 0 0 0 1 0 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0</td> <td>0 0 0 1 0 0 0 0 0 0 1 1 0 0 1 1 0 0 1 1 0 0</td> <td>0 1 0 1 0 0 0 0 0 1 0 1 1 0 1 1 0 1 0 1 1 0 1 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0</td> <td>0 0 1 1 0 0 0 0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0</td>		TRIP_CNT[4]           TRIP_CNT_out[0]           TRIP_CNT_out[1]           TRIP_CNT_out[2]           TRIP_CNT_out[3]           TRIP_CNT_out[4]           TRIP_CNT_out[4]           TRIP_CNT_out[4]           TRIP_COGIC_1           TRIP_LOGIC_0           TSP[0]           TSP[0]           TSP[2]           O           TSP[2]           TSP[3]           TSP[4]           TSP[5]           TSP[6]           TSP[7]	0 0 1 0 0 0 0 0 0 0 1 0 0 1 1 0 1 0 1 0	0 1 1 0 0 0 0 1 0 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0 0 0 1 1 0 0 1 1 0 0 1 1 0 0	0 1 0 1 0 0 0 0 0 1 0 1 1 0 1 1 0 1 0 1 1 0 1 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 0 0 0 0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
IBD Windfor           ■ Verty Help           ■ LC         Reheat for the	Normality         CE from P2           Displays writikle:         Input (2)         Image and the second se		TRIP_CNT_out[0]           TRIP_CNT_out[0]           TRIP_CNT_out[0]           TRIP_CNT_out[2]           TRIP_CNT_out[3]           TRIP_CNT_out[4]           TRIP_CNT_out[4]           TRIP_LOGIC           TRIP_LOGIC_0           TRIP_LOGIC_0           TSP[0]           TSP[0]           TSP[2]           O           TSP[2]           TSP[3]           TSP[4]           TSP[5]           TSP[5]           TSP[7]           TSP_10]	0 0 1 0 0 0 0 0 0 0 1 1 0 1 1 0 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 0 1 1 0	0 1 1 0 0 0 0 1 0 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0 0 0 0 1 1 1 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 0	0           1           0           1           0           0           0           0           0           0           1           0           0           1           0           1           0           1           0           1           0           1           0           1           0           1	0 0 1 1 0 0 0 0 0 0 1 0 1 1 0 0 1 1 0 1 0 1 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
IBD Winther           ■ Verity Help           ■ LC         Rehvent for a processing of the procesing of the processing of the processing of the processing of the	Norting         CE from P2           Drigsdays weithlike:         Input Ø Reg Ø Output Ø           Original CE         Reduced from Training graph Steel vars           Warning         Image of the state of		TRIP_CNT[4]           TRIP_CNT_out[0]           TRIP_CNT_out[1]           TRIP_CNT_out[2]           TRIP_CNT_out[3]           TRIP_CNT_out[4]           TRIP_CNT_out[4]           TRIP_CNT_out[4]           TRIP_COGIC_0           TRIP_LOGIC_0           TRIP_LOGIC_out           TSP[0]           TSP[0]           TSP[2]           TSP[3]           TSP[4]           TSP[6]           TSP[6]           TSP[7]           TSP[7]	0 0 1 0 0 0 0 0 0 1 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 0 0 1 0 0 1 0	0 1 1 0 0 0 0 1 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 0 1 0	0 1 0 1 0 0 0 0 0 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 0 0 0 0 0 1 1 0 0 1 1 0 0 1 1 0 1 1 0 0 1 1 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0
TBD VentWer           ■ Verty Holp           ■ Pact of Fig. RISING           ■ Pact of Fig. RISING           Normanies           Normanies           NO (           INI =           0.6 (           INI =           NO (	Northold         CF from P2           Design/ymg writibile:         Input ?         Reg ?         Output ?           Original CE         Reduced from Timing graph Steed vars         Warning         Interference         Interfere         Interfere         Inter		TRIP_CNT_out[0] 1 TRIP_CNT_out[0] 1 TRIP_CNT_out[1] 0 TRIP_CNT_out[2] 0 TRIP_CNT_out[3] 0 TRIP_LOGIC_1 0 TRIP_LOGIC_1 0 TRIP_LOGIC_0UT 0 TRIP_LOGIC_0UT 0 TSP[0] 1 TSP[3] 1 TSP[4] 1 TSP[5] 1 TSP[5] 1 TSP[5] 1 TSP[7] 0 TSP_1[0] 1 TSP_1[1] 0 TSP_1[2] 0	0           0           1           0           0           0           0           0           0           0           0           0           0           1           0           1           0           1           0           1           0           1           0           1           0           1           0           1           0           1	0 1 1 0 0 0 0 1 1 1 1 1 1 1 0 1 1 0 1 1 0 1 1 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0           0           0           0           0           0           0           0           0           0           0           0           1           0           1           0           1           0           1           0           1           0           1           0           1           0           0           0           0           0           0           0           0           0           0	0       1       0       1       0       0       0       0       1       0       1       0       1       0       1       0       1       0       1       0       1       0       1       0       1       0       1       0       1       0       0       0	0           0           1           1           0           0           0           0           0           0           0           0           1           0           1           0           1           0           1           0           1           0           1           0           1           0           1           0           1           0           1
IBD VentWer           ■ Venty Holp           ■ PLC         Rehmet K( • • • • • • • • • • • • • • • • • •	Norting         €E from P2           Displaying weithink:         Input [2]           Original CE         Reduced form           Things problem         Stoced vars           Warning         Input problem           PV_OUT         SP           PR         0000           PR         0000      <		TRIP_CNT_0ut[0] 1 TRIP_CNT_out[0] 1 TRIP_CNT_out[0] 1 TRIP_CNT_out[2] 0 TRIP_CNT_out[3] 0 TRIP_CNT_out[4] 0 TRIP_LOGIC_1 0 TRIP_LOGIC_1 0 TRIP_LOGIC_0ut 0 TRIP_LOGIC_out 0 TSP[0] 1 TSP[1] 0 TSP[2] 0 TSP[3] 1 TSP[6] 1 TSP[6] 1 TSP[0] 1 TSP[10] 1 TSP_1[0] 1 TSP_1[1] 0 TSP_1[2] 0 *	0 0 1 0 0 0 0 0 0 0 1 1 0 0 1 1 0 1 0 1	0           1           0           0           0           0           0           0           0           0           0           1           0           1           1           0           1           0           1           0           1           0           0           1           0           0           0	0       0       0       0       0       0       0       0       1       0       1       0       1       0       1       0       1       0       1       0       1       0       1       0       0       0       0       0       0       0       0	0         1         0         1         0         0         0         0         1         0         1         0         1         1         0         1         0         1         0         1         0         1         0         0         0         0         0         0         0	0 0 1 1 1 0 0 0 0 0 1 1 1 1 0 1 1 0 1 1 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0

Figure 4. FBD Verifier: A CASE tool for automatically translating FBD into Verilog programs: (a) automatic translation of a Verilog program, (b) SMV verification results—a counterexample, and (c) the counterexample's timing graph. Without proper visual support, counterexample analysis is boring and potentially error-prone, even for people with technical knowledge of model checking.

execution of Cadence SMV as one of NuSRS 2.0's pop-up verification menus. In Figure 2, the windows on the right illustrate that domain experts can perform all the verification activities without having to know separate commands for invoking Cadence SMV. The properties to be proved, however, couldn't have been automatically generated, so we encoded temporal-logic formulas in close consultation with nuclear engineers. Such properties, however, rarely change, although details on requirements or FBD design might change. We also performed Cadence SMV model checking on two subsystems: BP (Bi-stable Processor) and CP (Coincidence Processor). We detected 25 errors, including an incorrect specification in BP. Most errors were omissions in the specification. Although a few mistakes were introduced during formal specification, we discovered and fixed them relatively quickly. We report on the official verification results for a preliminary version of BP in previous work.<sup>7</sup>

During design, we applied Cadence SMV

model checking and VIS equivalence checking on FBD programs. Whereas the former examines whether the FBD programs meet required properties, the latter determines behavioral equivalence between two FBD revisions. For Cadence SMV model checking, we first defined FBD's semantics as a state transition system and developed rules to generate semantically equivalent Verilog programs. Using model-checking techniques, we identified 13 distinct types of errors in the FBD programs and detected several incidents of incorrect FBD logic.<sup>8</sup>

To assist FBD design verification, we developed the FBD Verifier (see Figure 4a). This tool reads FBD programs in standard XML format from the PLC vendor's engineering tools (Figure 4a, left) and translates them into equivalent Verilog programs (Figure 4a, right). We didn't want to overwhelm domain experts with unnecessary details; nevertheless, the tool allows line-by-line comparison to give regulatory personnel and domain experts confidence that the translation is correct. Most domain experts would simply click buttons at the bottom to perform model checking without bothering with FBD and Verilog syntax details. Unfortunately, Cadence SMV often generates counterexamples with excessively primitive details (see Figure 4b). However, the Verilog code in the main window was highly useful for analyzing such counterexamples.

More important, domain experts will likely refuse to use formal methods if they have to manually perform such analysis. So, we developed a feature where users could enter arbitrary expressions and visually display how values change in a manner similar to the timing graph in Figure 4c. Users can choose to display only their items of interest. They can combine existing entries in the timing graph and display how those entries change values in the counterexample. Using the visualization tool, verification personnel can easily understand why model checking failed.

We also used the VIS verification system to determine behavioral equivalence between the two successive FBD revisions. Although VIS accepts Verilog as input, it offers no graphical interface, and the results only partially display relevant information. Existing VIS output is similar to that in Figure 5b (see the next page). To many who are not experts on formal methods, it simply says two Verilog programs exhibited different behavior after seven states but offers no useful insights as to why. It displays only partial information necessary to accurately understand the full scenario. Even a system output display, shown in the sixth state, isn't intuitive. Most nuclear engineers found the information in Figure 5b totally inadequate. However, with the VIS Analyzer tool we developed, engineers not only can compare two Verilog designs side-by-side (see Figure 5a) but also can click the Result Table tab to display the equivalence-checking results in an easily understandable format (see Figure 5c). A recent case study demonstrated that the behavioral-equivalence checking was effective.<sup>9</sup>

#### Safety Analysis

Fault tree analysis (FTA) is the most common safety analysis technique; the theory is mature, and the practice is well established for sequential source codes such as C. Developers usually perform FTA manually, using fault tree templates that illustrate potential failure modes. Unfortunately, no FTA template existed for NuSCR specification and FBD nodes, so we developed a set of templates to capture potential failure modes of the NuSCR language constructs<sup>10</sup> and FBD blocks.<sup>11</sup> Figure 6 (see page 49) shows a fault tree template for the AND function block. This template consists of fault events and cause/effect events. The cause/ effect events denote fault propagation and help analysts understand the logical operation. Our project partner, an instrumentation and control research group in a nuclear-engineering department, performed fault tree analysis, improved template definitions, and published the final FTA results.<sup>12</sup> Although safety analysis is mandatory in nuclear applications, this application could become optional for other domains.

e developed many of the tool prototypes as the need arose, while the project was in full swing. So, we plan to integrate all the tools, from requirements analysis to design. Most domain experts strongly prefer an integrated development and verification environment where analysis happens behind the scenes and results are displayed, visually if possible, in a language familiar to them. Such languages might vary from one domain to another.

Finally, regardless of technical advances in formal methods, testing will likely always remain an essential component. FBD testing technique is relatively undeveloped. We're developing theories on FBD testing measures so that developers and regulatory bodies can assess the adequacy of testing FBD quantitatively with proper tool support.

#### Acknowledgments

Konkuk University's faculty research fund supported this work in 2008.

Automatic Vis Equivalence Checker	r" 17 🛛	Automatic Vis Equivalence Checker
Verilog sources Result Result Table		Eile <u>R</u> un <u>H</u> elp
Best Verilog 1	Verilog 2	Verilog sources Result Result Table
WC2007TaVhomeW/Skis-2 Revembas/DPS/EDD Verifienth V Pretrin Manus	C1/C2007TaV/homel//Skie.2 @examples/DDSEDD_Verifienth_Y_Pretrin_Mechu	VALUET AV
cypedef enum (30, 31) th X Pretrip state;	typedef enum (30, 31, 32) th X Pretrip state;	
cypedef enum (TO, T1, T2, T3, T4, T5, T6, T7,	typedef enum {T0, T1, T2, T3, T4, T5, T6, T7,	Goes to state 1:
28, T9, T10, T11, T12, T13, T14, T15, T16,	T8, T9, T10, T11, T12, T13, T14, T15, T16,	state: S1
(17, T18, T19, T20) timer_state;	T17, T18, T19, T20) timer_state;	timer\$NTK2:T1
define k_Pretrip_Setpoint 30	define k_Pretrip_Setpoint 30	timer:T1
define k_X_Pretrip_Hys 10	define k_X Pretrip_Hys 10	On input:
- decine x_rrip_berey 20	// deline x_rrip_berey 20	f_X<0>:0
		f X<1>:1
/ th_X_Pretrip module accule th X Pretrip(clk, f X. th X Pretrip).	module th X Pretrip(clk, f X, th X Pretrip).	f_x<2>:1
	and an	f x<3>:1
input clk;	input clk;	f X<4>:1
.nput[U:6] f_X;	unput[U:6] f_X; output th X Pretrip:	f X<5>:0
	in the second seco	f X<6>:1
/integer wire f_X;	//integer wire f_X;	
vire th X Pretrip;	wire th X Pretrip:	Goes to state 2:
P/		timerSNTK2:T2
:h_X_Pretrip_state reg state;	th_X_Pretrip_state reg state;	timer.m2
timer state reg timer;	timer state req timer;	-On impute
		On input:
initial state = S1;	initial state = 30;	Sonemanged
initial timer = TO;	initial timer = TO;	
		Goes to state 3:
<pre>issign th X Pretrip = (state== \$0 &amp;&amp; f X &lt;= ) }</pre>	wine Cand a la	timer\$NTK2:T3
(state==30 && f X >	wire Cond b 1;	timer: T3
k_Pretrip_Setpoint - `k_X_Pretrip_Hys 44	wire Cond_c_1;	On input:
imer == T5)?0:	agains Cond a 1 = (f Y b= 'b Dystyin Saturint);	<unchanged></unchanged>
'k Pretrip Setpoint - 'k X Pretrip Hys 44	assign Cond b 1 = ((f X >=	
cimer 1= T5)?1:	<pre>`k_Pretrip_Setpoint) &amp;&amp; (timer == T5));</pre>	Goes to state 4:
(state==S1 && f_X <	<pre>//assign Cond_c_l = (f_X &lt; `k_Pretrip_Setpoint )</pre>	timer\$NTK2:T4
		timer: T4
	T I	On input:
atty		<unchanged></unchanged>
		Goes to state 5:
A)		timerSNTK2:T5
		timer: T5
		On input:
		<unchanged></unchanged>
Automatic Vis Equivalence Checker	•°0° 🛛	Goes to state 6:
le <u>R</u> un <u>H</u> elp		state\$NTK2:30
Denut Denut Denut Table		state: S2
Verling sources Result Result Table		th Prev X Pretrip\$NTK2:0
# state input File1Output	File2Output File1State File2State	th Prev X Pretrip:0
J Initial Initial	Initial S1 1 TO S0 1 TO	On input:
61 1	1 S11T1 S11T1	< Inchanged>
61 1	1 S1 1 T2 S1 1 T2 1 S1 1 T2 S1 1 T2	· · · · · · · · · · · · · · · · · · ·
61 1	1 S11T4 S11T4	Goes to state 7.
61 1	1 \$11 T5 \$11 T5	timerCimy2.m0
61 0	0 80 0 T5 82 0 T5	timer, m0
E2 0	0 \$0 0 TO \$2 0 TO	
52 0		On input:
52 U 52 1		t_X<3>:U
52 U		III±_X<6>:0
ady		
ady		Vietness Vom servertig 22 service 2 set
2 02 0 52 1 ady \$)		Networks are NOT sequentially equivalent.
22  0  52  1  atty		Networks are NOT sequentially equivalent. vis> vis release 2.0 (compiled Sat Jun 14 12:02:36 200
ady		
arty		Networks are NOT sequentially equivalent. Vis> vis release 2.0 (compiled Sat Jun 14 12:02:36 200 <u>vis&gt; vis&gt; vis&gt; vis&gt; vis&gt; is&gt; is&gt; is&gt; is&gt; is&gt; is&gt; is&gt; is&gt; is&gt; </u>

Figure 5. VIS Analyzer: A CASE tool for seamless execution and visualization of VIS: (a) two Verilog programs, (b) VIS equivalence checking results, and (c) the result table. It's important to reduce the semantic gap between "raw data" and "domain knowledge" whenever possible.

#### References

- K.L. Heninger, "Specifying Software Requirements for Complex Systems: New Techniques and Their Application," *IEEE Trans. Software Eng.*, vol. 6, no. 1, 1980, pp. 2–13.
- J. Yoo et al., "A Formal Software Requirements Specification Method for Digital Nuclear Plants Protection Systems," J. Systems and Software, vol. 74, no. 1, 2005, pp. 73–83.
- S. Cha, "Pet Formalisms versus Industry-Proven Survivors: Issues on Formal Methods Education," J. Research and Practice in Information Technology, vol. 32, no. 1, 2000, pp. 39–46.
- M.P.E. Heimdahl and N.G. Leveson, "Completeness and Consistency in Hierarchical State-Based Requirements," *IEEE Trans. Software Eng.*, vol. 22, no. 6, 1996, pp. 363–377.
- J. Yoo et al., "Synthesis of FBD-Based PLC Design from NuSCR Formal Specification," *Reliability Eng. and System Safety*, vol. 87, no. 2, 2005, pp. 287–294.

- US Nat'l Research Council, Digital Instrumentation and Control Systems in Nuclear Power Plants: Safety and Reliability Issues, Nat'l Academy Press, 1997.
- J. Cho, J. Yoo, and S. Cha, "NuEditor—a Tool Suite for Specification and Verification of NuSCR," Proc. 2nd ACIS Int'l Conf. Software Eng. Research, Management, and Applications (SERA 04), IEEE Press, 2004, pp. 298–304.
- J. Yoo, S. Cha, and E. Jee, "A Verification Framework for FBD Based Software in Nuclear Power Plants," *Proc. 15th Asia Pacific Software Eng. Conf.*, IEEE Press, 2008, pp. 385–392.
- 9. J. Yoo, S. Cha, and E. Jee, "Verification of PLC Programs Written in FBD with VIS," *Nuclear Eng. and Technology*, Feb. 2009.
- T. Kim, J. Yoo, and S. Cha, "A Synthesis Method of Software Fault Tree from NuSCR Formal Specification Using Templates," *J. Korea Inst. Information Scientists* and Engineers, vol. 32, no. 12, 2005, pp. 1178–1192 (in Korean).



Figure 6. A fault tree template for the AND function block. It illustrates how failure can occur and what dependencies exist among potential causes.

- Y. Oh et al., "Software Safety Analysis of Function Block Diagrams Using Fault Trees," *Reliability Eng.* and System Safety, vol. 88, no. 3, 2005, pp. 215–228.
- G.-Y. Park et al., "Fault Tree Analysis of KNICS RPS Software," Nuclear Eng. and Technology, vol. 40, no. 5, 2008, pp. 397–408.

For more information on this or any other computing topic, please visit our Digital Library at www.computer.org/csdl.

# About the Authors



Junbeom Yoo is an assistant professor in Konkuk University's Department of Computer Science and Engineering. His research interests include requirements engineering and formal methods. Yoo has a PhD in computer science from the Korea Advanced Institute of Science and Technology. Contact him at jbyoo@konkuk.ac.kr.

**Eunkyoung Jee** is a PhD candidate at the Korea Advanced Institute of Science and Technology. Her research interests include software testing and safety-critical software. Jee has an MS in computer science from the Korea Advanced Institute of Science and Technology. Contact her at ekjee@dependable.kaist.ac.kr.







**Sungdeok (Steve) Cha** is a professor in Korea University's Computer Science and Engineering Department. His research interests include software safety and computer security. Cha has a PhD in information and computer science from the University of California, Irvine. Contact him at scha@korea.ac.kr.